

DPA26BZ01-NV002
Photonic-Electronic Panels for Multi-chip Integration
Frequently Asked Questions (FAQs)

1. Does the PEPI program prioritize the evaluation of integrated substrate-level survivability (HEMP/EMP resilience) as a metric for 3D photonic-electronic panel integration?
A: The PEPI program Phase I prioritizes designing a platform that provides a credible pathway to meeting the eventual Phase II metrics. Integrated substrate-level survivability (HEMP/EMP resilience) can be an added benefit of a proposed design, but the priority is the requirements (routing, pitch, link loss, and component count, etc.) listed in the Phase II metrics table.

2. In terms of qualifying FAU detachability—are metrics such as attach repeatability, attachment to the panel's surface versus side, footprint, and direct connections to multilayers prioritized?
A: The FAU detachability requirement is meant to encourage the design of a repeatable, reusable interface with low loss, avoiding the complexity and inflexibility of actively aligned, permanent I/O mounts. There is no requirement on footprint or surface vs side attachment, but it must couple >16 fibers into the panel.

3. Is the interconnect pitch a requirement for both OI-1 and OI-2? Is this pitch defined for a 1D grid, or a square 2D grid?
A: The interconnect pitch is a requirement for the OI-1 and it is for a square 2D grid.

4. Can performers implement back-end-of-the-line modification to the commercial ICs? Is minimal modification preferred?
A: The panel design should emphasize compatibility with commercial IC's with minimal modification which aligns with the program goal of designing an adaptable and practical platform for integrating EICs and PICs together. Phase II requires a packaging compatibility report to outline methods and constraints for bonding/coupling to the panel systems.