DARPA-PA-25-07-01 Fast and Curious
Frequently Asked Questions (FAQs)
as of 02/05/2026

18Q: Is there a preference for applications geared more toward AI as opposed edge computing for SWaP-constrained platforms

18A: No

17Q: Is technology based on two dimensional materials that can hit performance metric, but is not currently scalable to wafer size, within scope?

17A: Yes

16Q: Is there interest in implementing other types of computational circuits, such as matrix multiplications

16A: As discussed in the DO, it is acceptable to implement circuits of equivalent complexity and relevance to the DoW as the ones specified in the program metrics.

15Q: Will there be any assistance in providing the equipment needed to test the high speed switching required for the program?

15A: No, each performer is required to demonstrate the performance required by the program using equipment provided by their team.

14Q: If we develop phase 1 prototypes that meet the performance metrics, but due to their size cannot yet satisfy the temporal metrics, would it be acceptable to demonstrate compliance with the temporal metrics through validated modeling? With the understanding that they will be achieved at scale.

14A: No. The program metrics need to be satisfied with direct experimental measurements.

13Q: Are analog devices within the scope? Is the focus fully on digital?

13A: No. Analog devices are not in scope of this program.

12Q: Is the lateral size and/or temperature of operation important for meeting the program target?

12A: Cryogenic approaches are not in-scope. There are no explicit requirements on the lateral dimensions, so long as the performance satisfies the program metrics.

11Q: What is the level of importance of moving away from rare earth materials?

11A: This is not a consideration for this program.

10Q: Is choosing approaches that do not use multiferroic materials a non-starter for this program?

10A: No. Except devices requiring cryogenic cooling, approaches with sufficient evidence supporting the feasibility of achieving program goals will be considered.

9Q: Is volatile logic within scope: How great of priority is memory-in-logic?

9A: Yes, volatile logic is within scope of this program. Memory-in-logic is of interest to this program. If the logic is volatile, it is preferred that the proposed work can enable highly integrated memory and logic without latency.

8Q: Is the proposed technology required to be CMOS compatible?

8A: No

7Q: If a Milestone requires 90% efficiency for a $200k payment but I only hit 85%, can the government withhold the amount, leaving me to absorb the costs of that milestone? Is my understanding of this financial risk correct?"

7A: Yes

6Q: Are superconducting logic / device-physics approaches aligned with the Fast and Curious DO scope?

6A: No

5Q: Are there any non sensitive suggestions you may have on the kinds of roles or capabilities (e.g., multiferroic / magnetoelectric stack development, thin film deposition and characterization, pilot scale process lines) that would be most relevant and useful to the Fast and Curious technical objectives?

5A: No. Please refer to the program goals in the solicitation for the capabilities sought after by the program.

4Q: Are materials focused small businesses are encouraged to participate as part of teaming arrangements on this program?

4A: Yes

3Q: Is cryogenic logic in scope?

3A: No

2Q: Will the program permit FFRDCs to be on the performer team?

2A: Yes. Please see Section III of the DO for details.

1Q: Would a proposed solution that develops cryogenic ultra-low power electronics, including novel post-SFQ circuits, be considered to be "in scope"?

1A: No