Fast and Curious

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Information Session

February 4, 2026

Revolutionize the transistor by mastering multiferroics

Multiferroics are a unique set of materials that exhibit two or more ferroic properties simultaneously, such as ferroelectricity and ferromagnetism

H1: The Fast and Curious Program will develop wafer-scale manufacturable fabrication techniques and new interfaces between ferroic materials that maximize transduction for a new class of low-energy, high-speed logic circuits

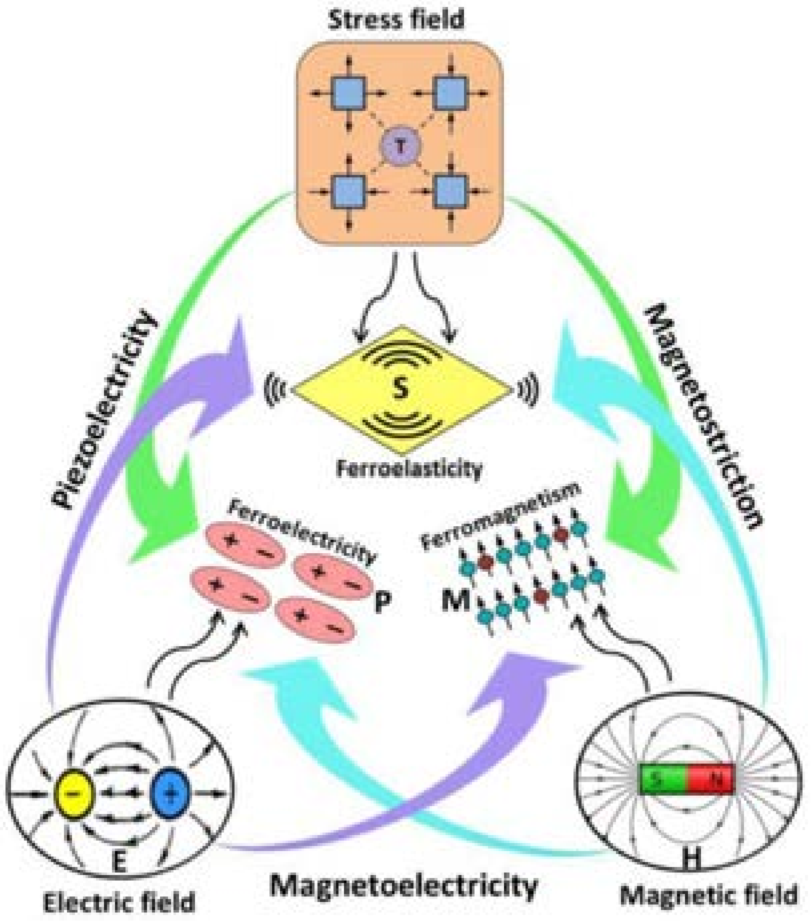
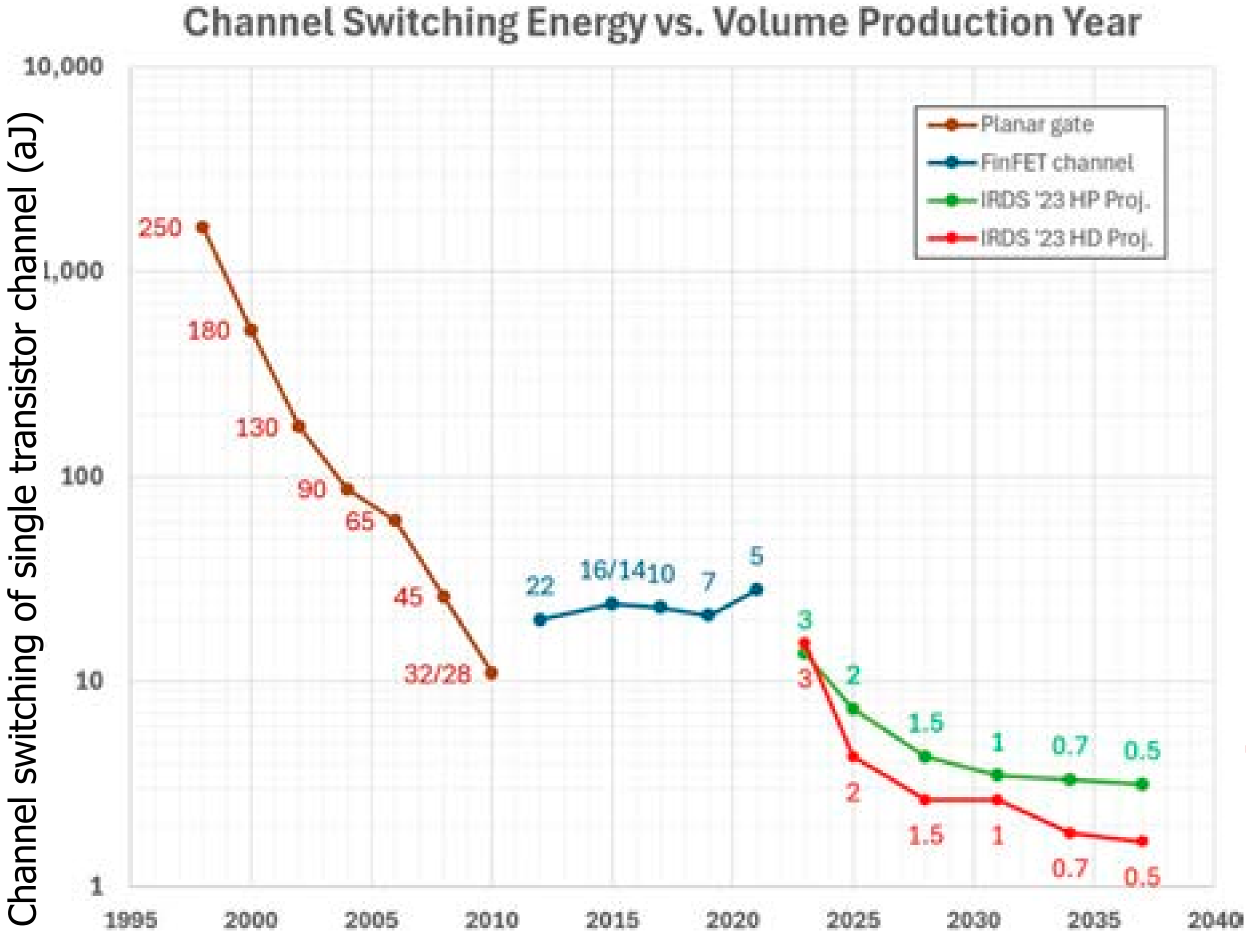


Figure from https://www.mdpi.com/2076-0825/5/1/9

H2: CMOS energy efficiency will hit the thermal noise floor



Thermal noise danger zone!!

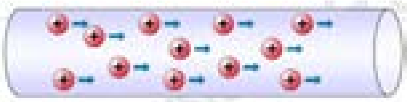
Program Goal: Demonstrate logic circuits with >100x greater energy efficiency

Michael P. Frank, Alexander J. Edwards; Industry perspective: Limits of energy efficiency for conventional CMOS and the need for adiabatic reversible computing. APL Electronic Devices 1(3) 030902 (2025)

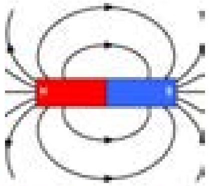
CMOS: Complementary metal–oxide–semiconductor
HD: High density
HP: High performance
IRDS: International Roadmap for Devices and Systems

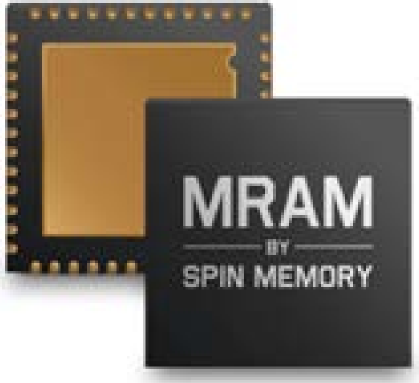
CMOS is fundamentally limited by its reliance on free charge

Free charge

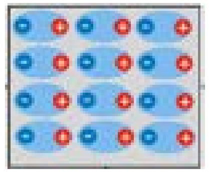


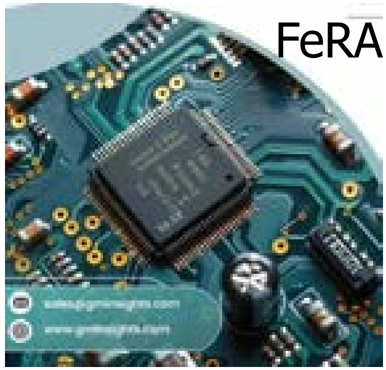
Magnetization





Polarization (Bound Charge)





FeRAM

Property/logic variable	**Charge (CMOS)**	**Collective spin or Polarization**	**Advantage over CMOS**
Physical constituents	Non interacting, single particle	Interacting, collective (10^5 spins/bit)	Dissipation does not scale with particle number
Thresholding	Set by thermal noise floor/subthreshold current	Set by coercive field	Lower switching voltage; No dissipation from leakage current
Stability	Required applied voltage	Stability against thermal fluctuations set by internal interaction energy	Non-volatile (radiation hard)

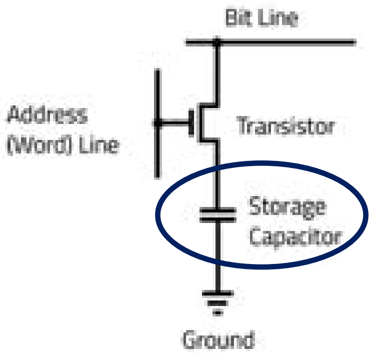
Ferroics are mature for memory and primed for extension to logic

CMOS: Complementary metal–oxide–semiconductor
FeRAM: Ferroelectric Random Access Memory
MRAM: Magnetic Random Access Memory

Logic circuits require gain for fan-out + speed and energy

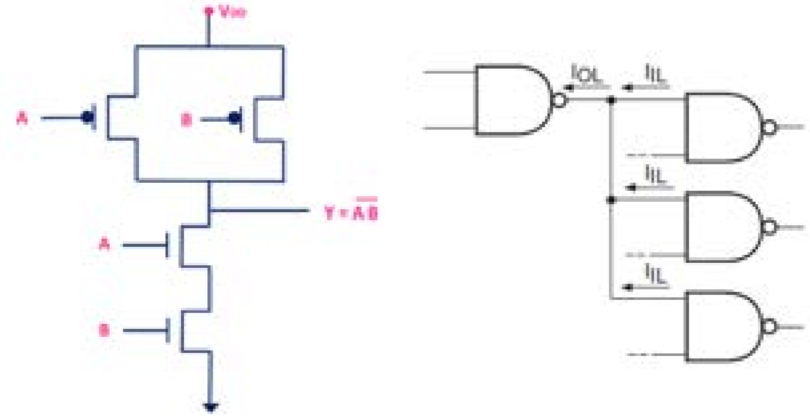
Unit Memory Cell is a 2-terminal device

Key criteria: Retention time, reliability, access speed

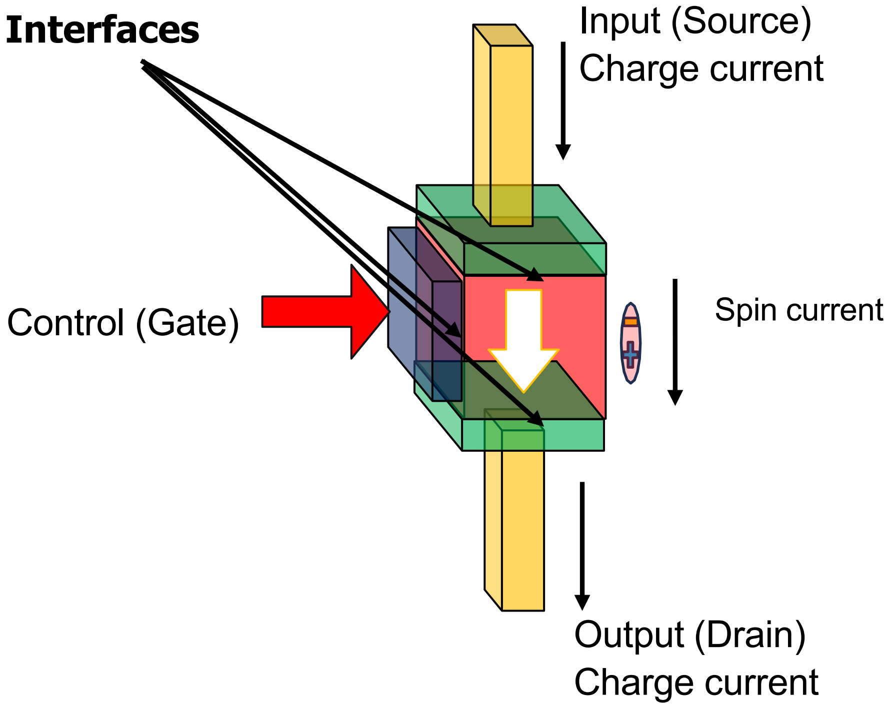


A Logic gate requires 3-terminal transistors

Key criteria: Switching speed, energy and fan-out

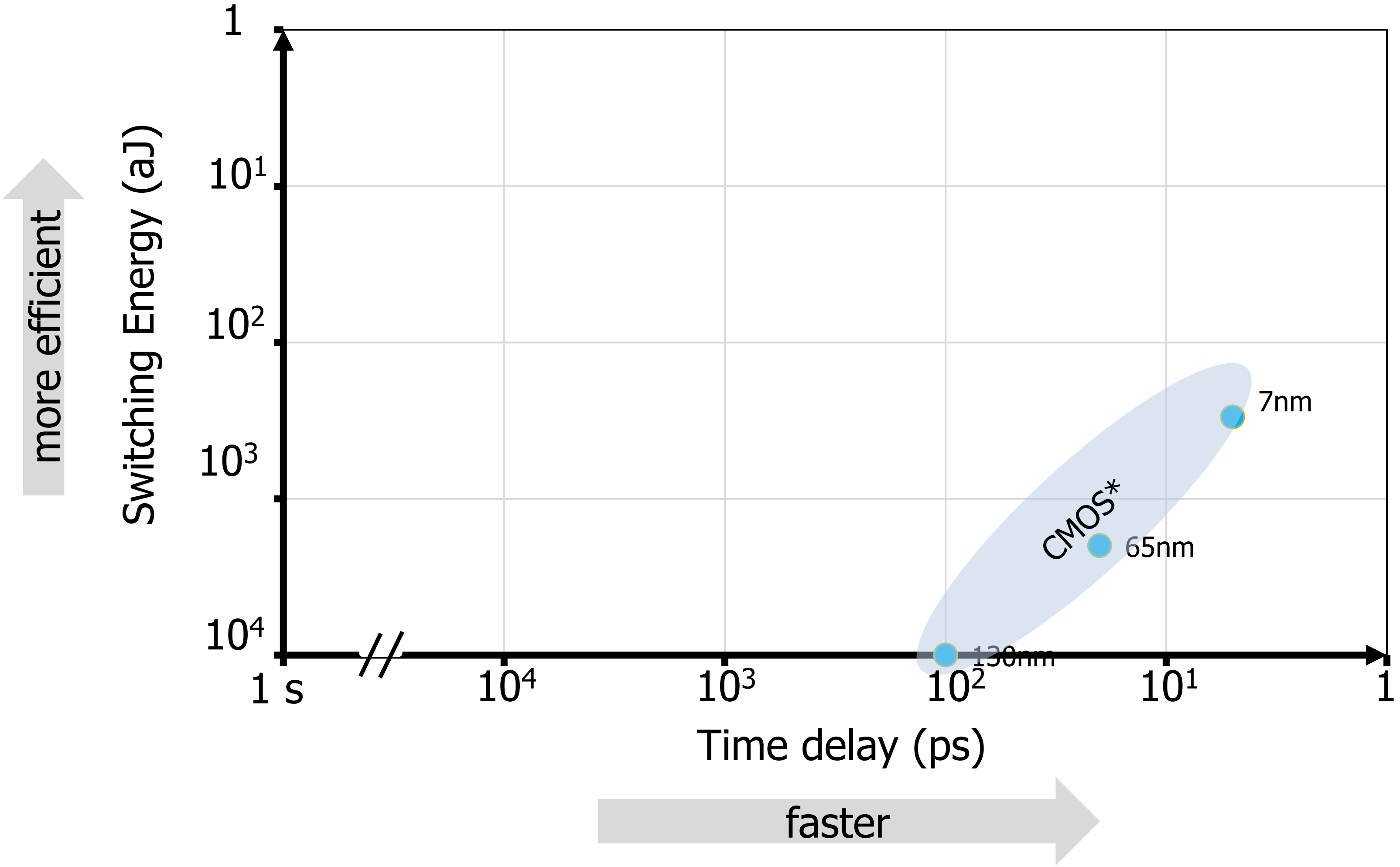


Multiferroic 3-terminal device



- Spin or Polarization based logic requires transduction
  - e.g., *magnetoelectric transduction* for spin-based logic
- *Multiferroic* materials enable transduction and gain

CMOS sets standard for switching time and energy

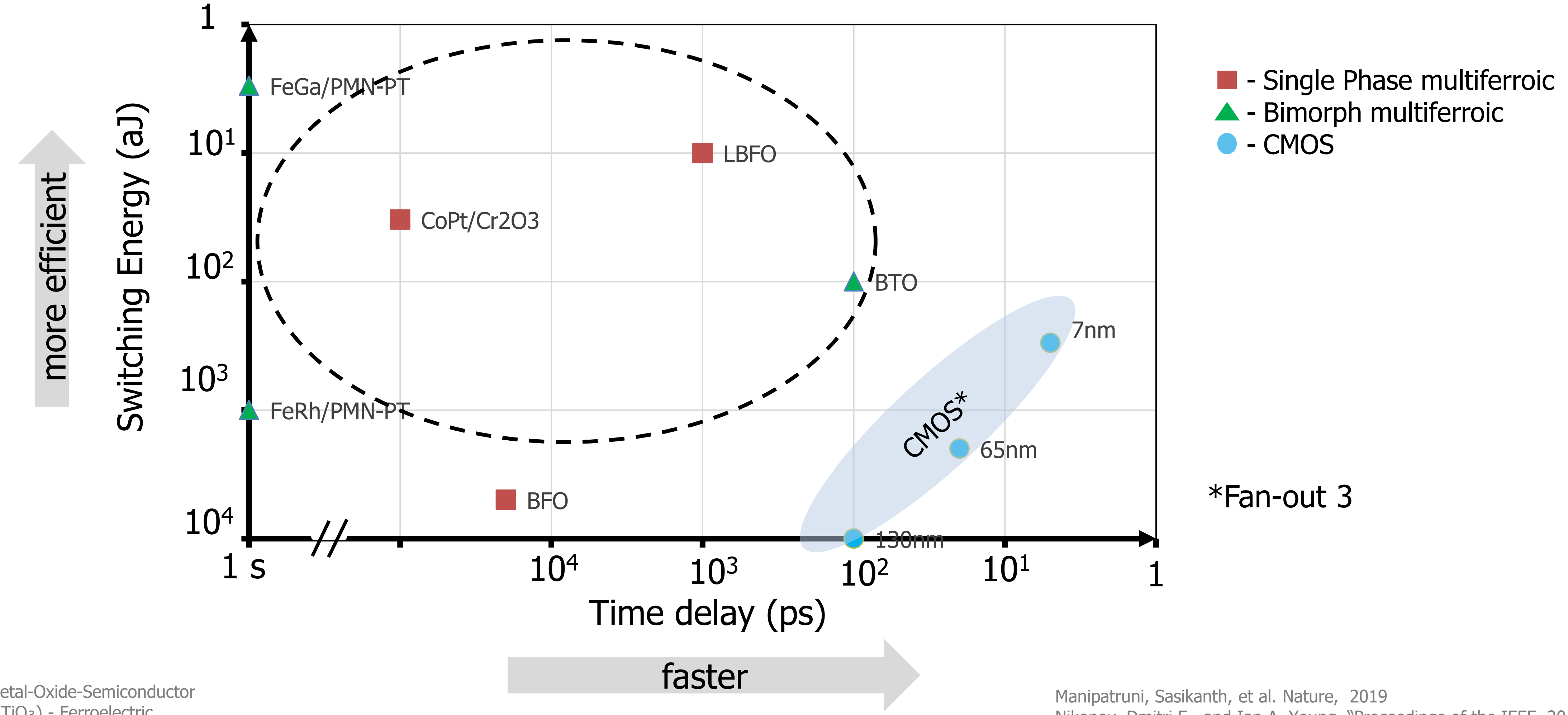


*Fan-out = 3

CMOS: Complementary Metal-Oxide-Semiconductor

Recent Multiferroics confirm low switching potential

but lag in fan-out and speed objectives

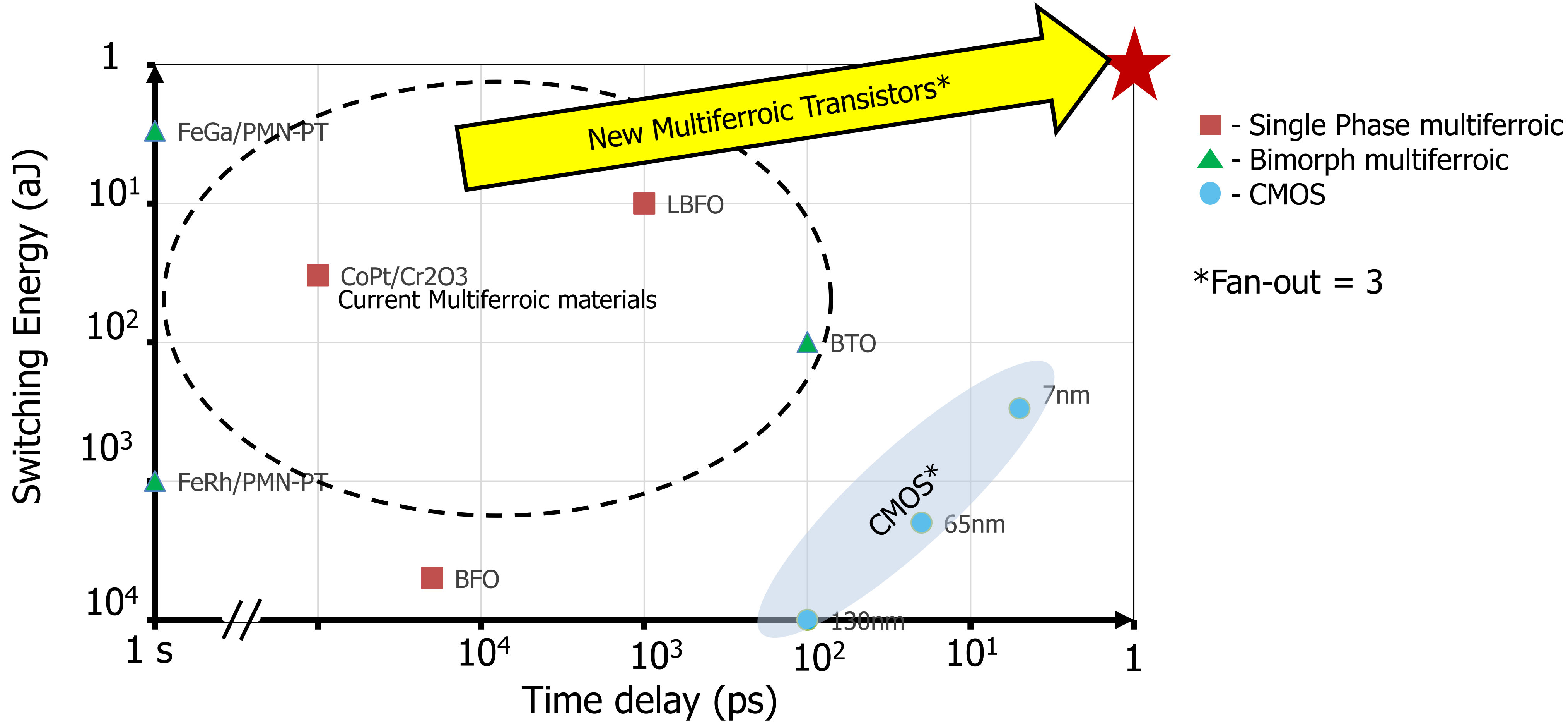


*Fan-out 3

CMOS: Complementary Metal-Oxide-Semiconductor
BTO: Barium Titanate ($BaTiO_3$) - Ferroelectric
BFO: Bismuth Ferrite ($BiFeO_3$) - Single-phase multiferroic
LBFO: Lanthanum-Doped Bismuth Ferrite ($La_xBi_{1-x}FeO_3$) - Single-phase multiferroic
FeGa: Iron–Gallium Alloy ($Fe_{1-x}Ga_x$) - Magnetostrictive
PMN-PT: Lead Magnesium Niobate–Lead Titanate - Ferroelectric

Manipatruni, Sasikanth, et al. Nature, 2019
Nikonov, Dmitri E., and Ian A. Young. "Proceedings of the IEEE, 2013
Parsonnet, Eric, et al.,Physical Review Letters, 2020
Prasad, Bhagwati, et al. Advanced Materials, 2020
Shi, Qiwu, et al., Nature Communications, Mar. 2022

Goal: Logic circuits beating CMOS in energy and speed



*Fan-out = 3

Combination of material exploration, modeling, device design, and processing needed to extend multiferroics to objective time delay and fan-out

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Technical challenges for achieving efficient transfer through and between ferroic materials

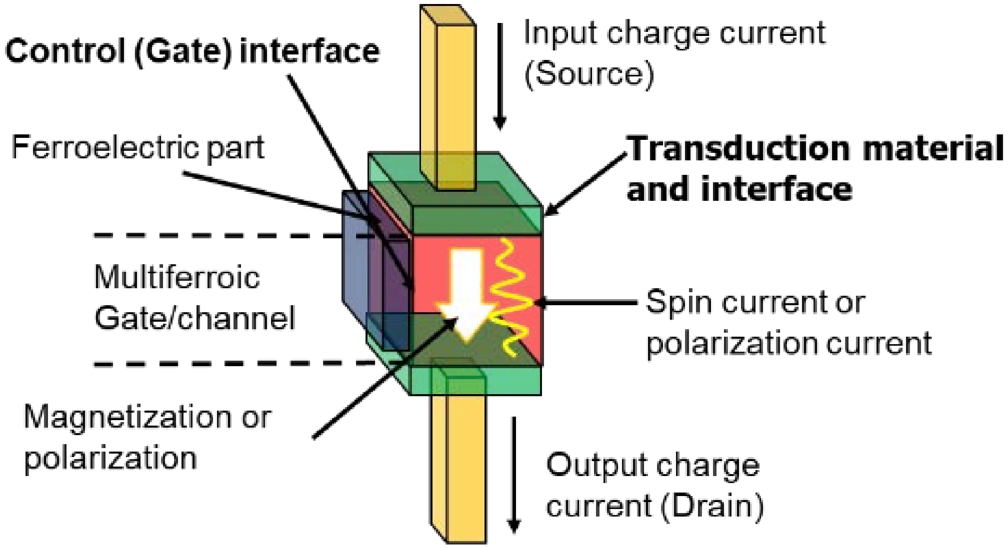
① **Gate** polarization switched by input voltage, inducing mechanical stress that is transduced through the **Interface** to the channel, inverting the phase of the **Channel's** spin or displacement current

A. High coupling for energy efficiency and fast switching: channel delay, $\tau = \frac{\pi}{(1+\kappa_G)\gamma\alpha_E E}$ = 1.2ps for $\alpha_E = 10^{-5}$

B. High quality interface with thin materials for speed and scalability: acoustic velocity 9 km/s => 9 nm enables 1ps

② Read-out of current induces large output voltage swing to drive 3 gates in next stage

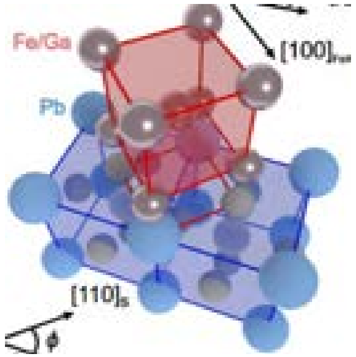
A. Requires efficient waveguiding through channel

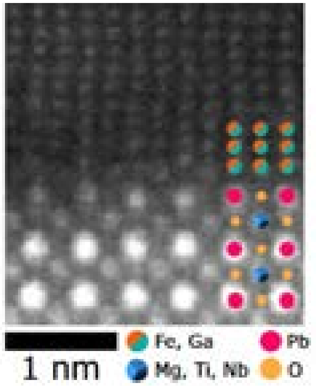


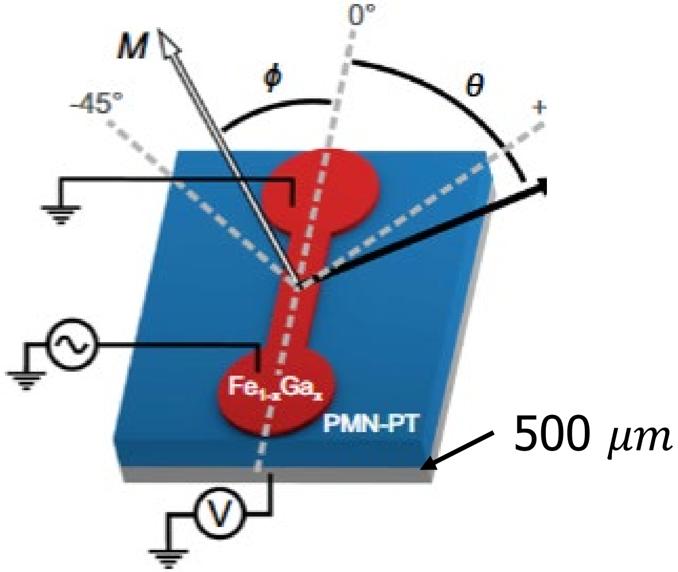
	① Switch energy per bit (aJ)	① Switching time delay (ps)	② Gate Voltage	② Output Voltage (Fan-out capability)
State of the Art (each from different demos, not from one device)	3	100	200mV	0.001 mV
Program Goal	1	1	<20 mV	>100 mV

α_E: converse magnetoelectric coupling

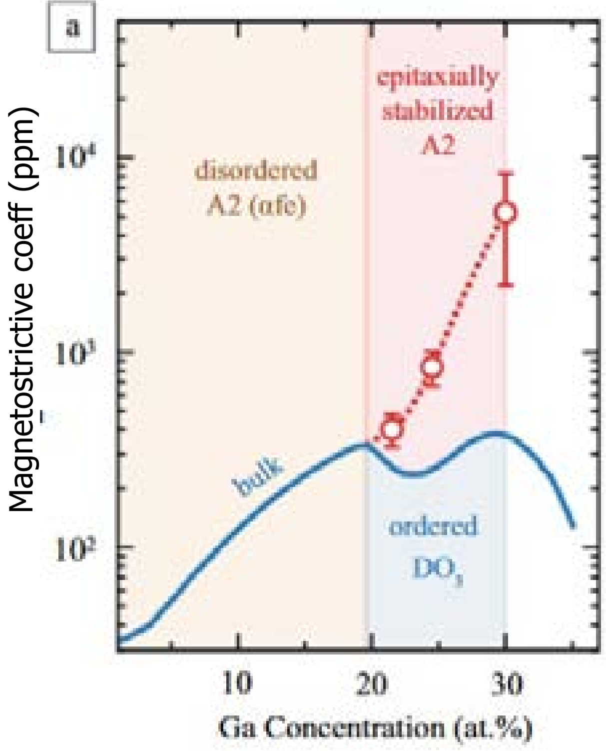
1A) High coupling for energy efficiency and fast switching



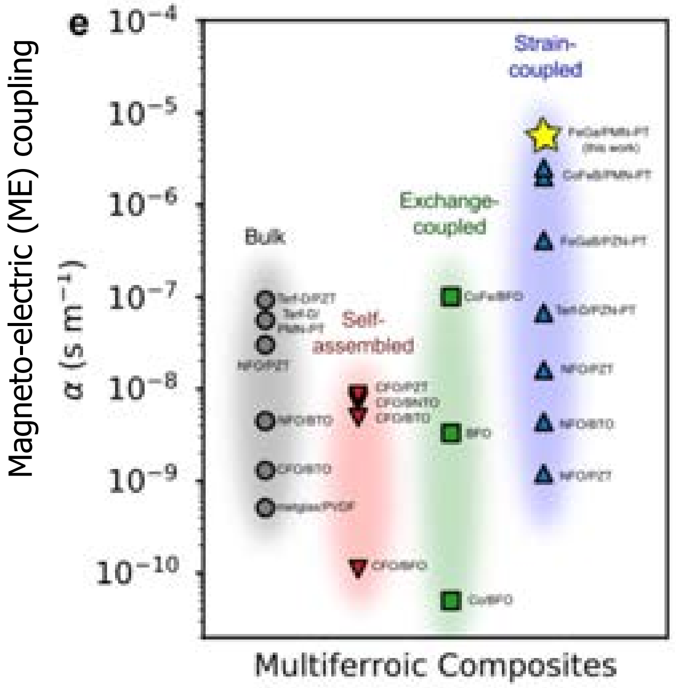




More Gallium enhances Magnetostrictive coeff



Strain-coupled Multiferroics are the Best



- The PMNPT transducer applies a mechanical torque on the magnet to switch dipole orientation
  - Larger the magnetostriction, larger the coupling coefficient, results in lower energy required to switch dipole
  - Interface quality and coupling directly affects both Time and Energy
- ME Coupling limited by interface quality (roughness, dielectric losses), microstructure (relative orientation of grains), crystallographic orientation, clamping losses, resistive losses from leakage currents

Achieved largest converse ME coupling to-date in FeGa/PMN-PT composite with thin FeGa on bulk PMNPT

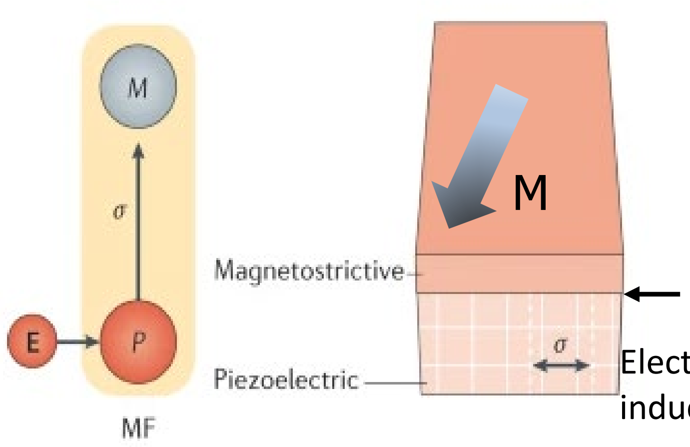
FeGa/PMN-PT data point: Meisenheimer, P. B., Bhave, Sunil, et al. Nature Comms 2021
Heron, John, presentation from ONR Workshop

ME: magnetoelectric

1B) High-quality interface with thin materials

Strain-mediated Coupling

3-Terminal Multiferroic Transistor



ϵ_p
strain-transfer efficiency η

Electrically induced strain

$$\alpha_E = \mu_0 \frac{\partial M}{\partial \sigma_m} \frac{\partial \sigma_m}{\partial \epsilon_m} \boldsymbol{\eta} \frac{\partial \epsilon_p}{\partial E}$$

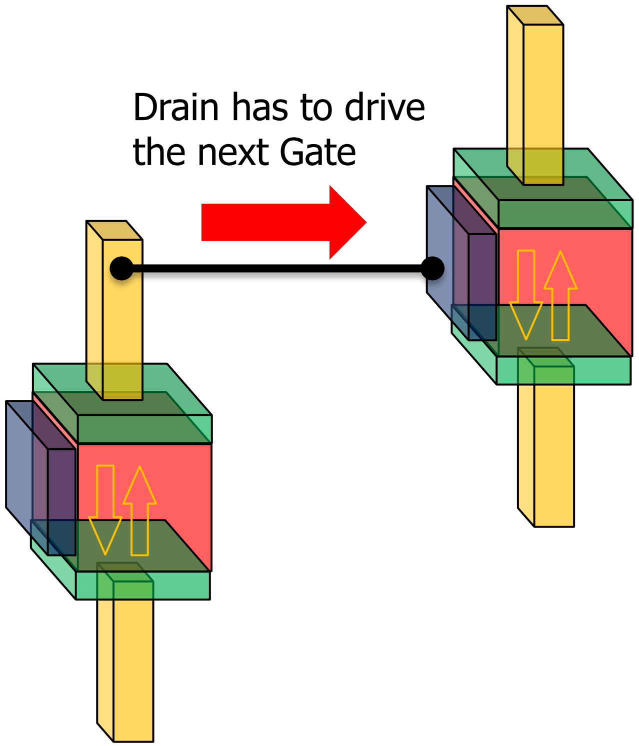
Insight: Strain-transfer efficiency **η** depends on the **quality of the interface**

Approach: Multilayer epitaxy through retrograde amorphous growth

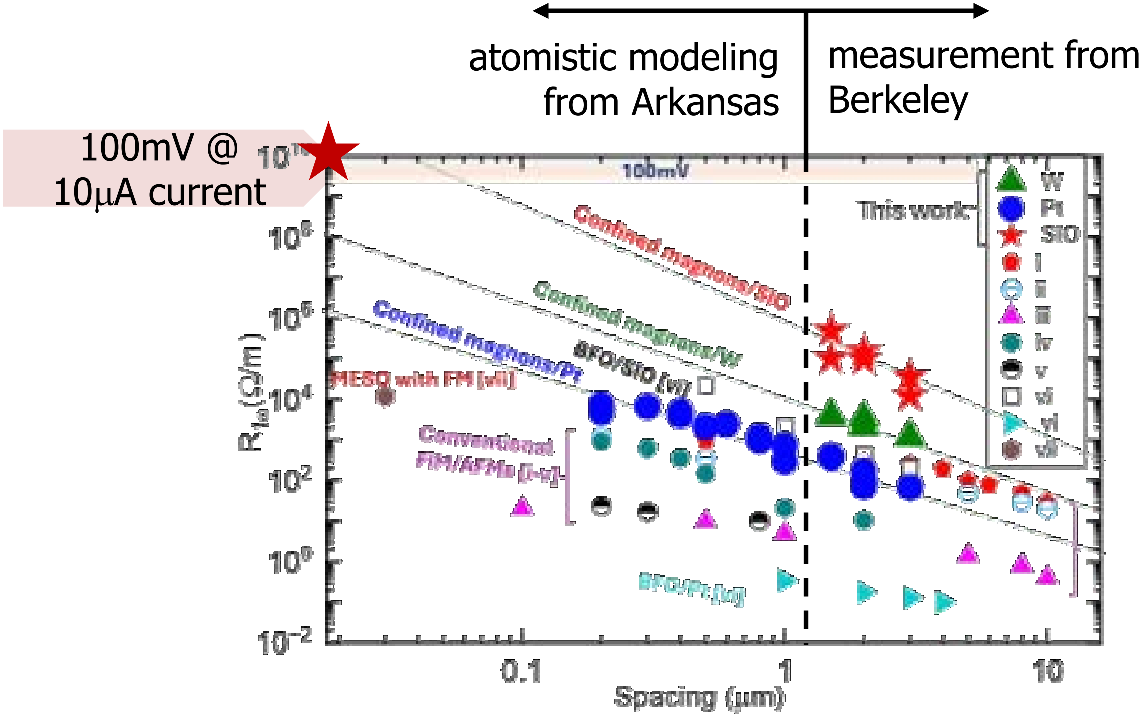
A perfectly engineered interface at wafer-scale has been demonstrated for a single ferroic layer

Fiebig, Manfred, et al. 2016

2) Efficient waveguiding through channel to enable fan-out



Drain has to drive the next Gate



atomistic modeling from Arkansas

measurement from Berkeley

100mV @ 10μA current

Husain, Sajid, et. al. arXiv:2503.23724

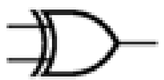
- Undesirable: intensity modulation of spin current
- Need: polarization reversal of spin current (collective flip of spins) to achieve large <u>Gain</u>

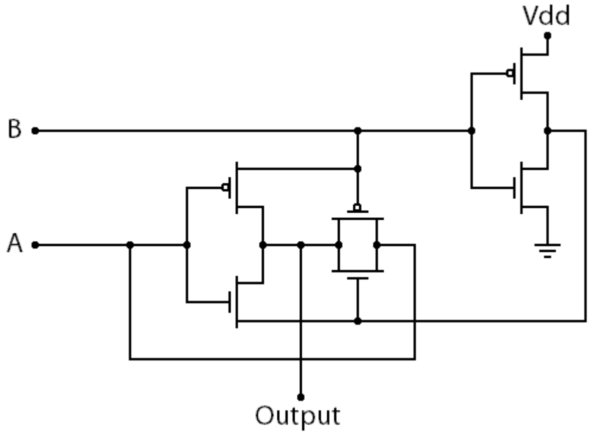
- Insight: improve spin transmission by **waveguiding spins across source-drain channel**

Theory extrapolation predicts 100mV output voltage at <100 nm channel length

Forcing the integration of materials development, processing, and device design by requiring teams to demonstrate full circuits

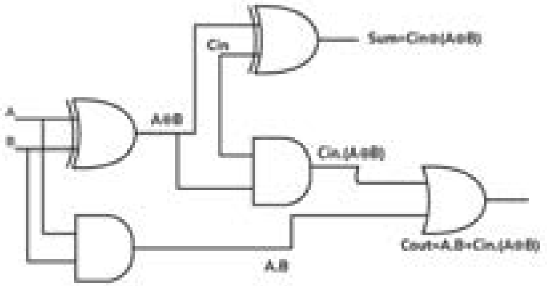
CMOS XOR

Symbol	A	B	Q
	0	0	0
	1	0	1
	0	1	1
	1	1	0
Q = A ⊕ B			



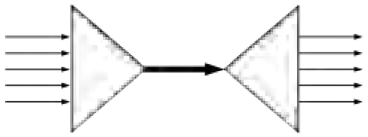
4 bit adder: 2 XOR, 2 AND, 1 OR

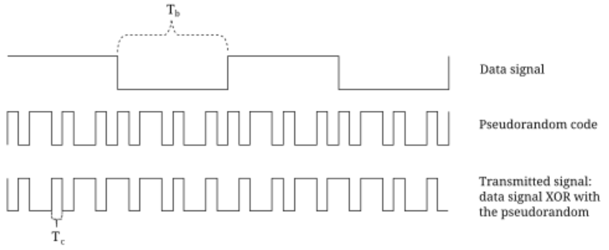
Inputs			Outputs	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



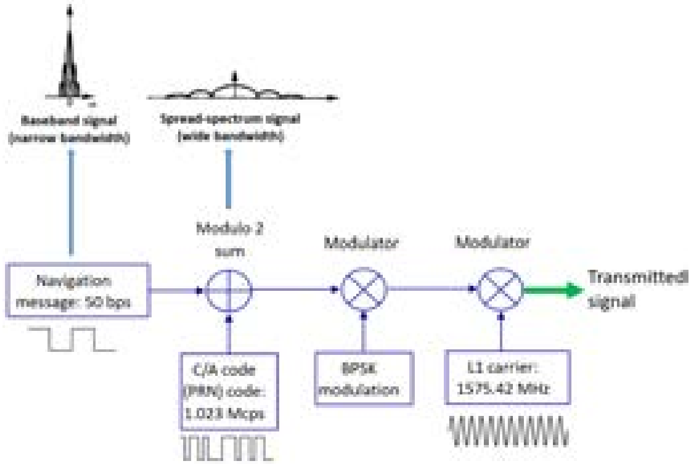
XORs are used in correlators

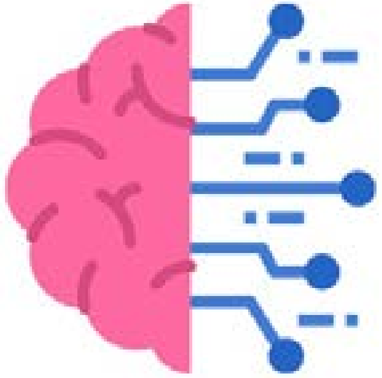
- E.g., Code-division multiple access CDMA





Correlators are used in GPS signal acquisition and AI





We will demonstrate multiferroic logic circuits, starting with XOR, Adder, and Correlator for scalable solutions

CMOS: Complementary Metal-Oxide-Semiconductor
XOR: eXclusive OR
CDMA: Code Division Multiple Access

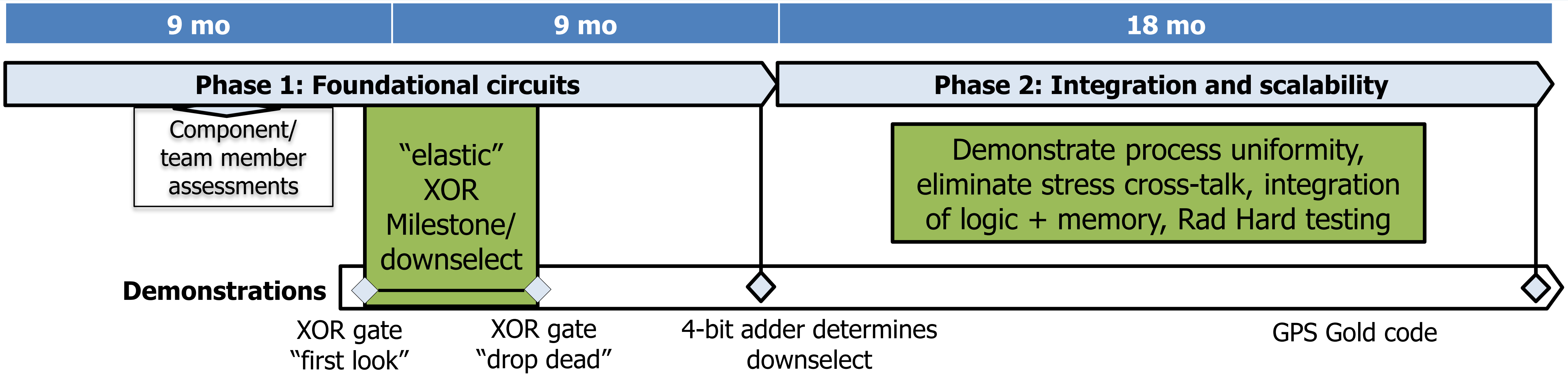
Program metrics

	Phase I	Phase II
Logic switch energy (aJ)	10	1*
Logic switch time delay (ps)	10	1
Fan-out	>1	>3*
Logic gate	XOR; 4-bit correlation	GPS Gold code (10^3 bits)

*Logic gate must be able to power a fan-out 3 node

XOR: eXclusive OR
ME: magnetoelectric

Active management converges to most promising solutions



At 9-12 months: Demonstrate XOR gate with some voltage swing with high- and low- noise margin. A milestone-based "elastic" metric enables an aggressive schedule that makes room for risky approaches, provides early opportunities to assess all teams and downselect.

Phase 1 downselect: By demonstrating a 4-bit adder, the performers will have achieved

1. 30 transistor sequential logic with fan-out = 3
2. Operation with no cross-talk

Phase 2 demonstrator: By demonstrating a GPS Gold Code correlator the performer will have achieved

1. Clocked Registers with non-volatile Memory-in-Logic!
2. A multi-level BEOL technology

XOR: eXclusive OR; BEOL: back end of line

If successful, impact goes beyond energy efficient transistor

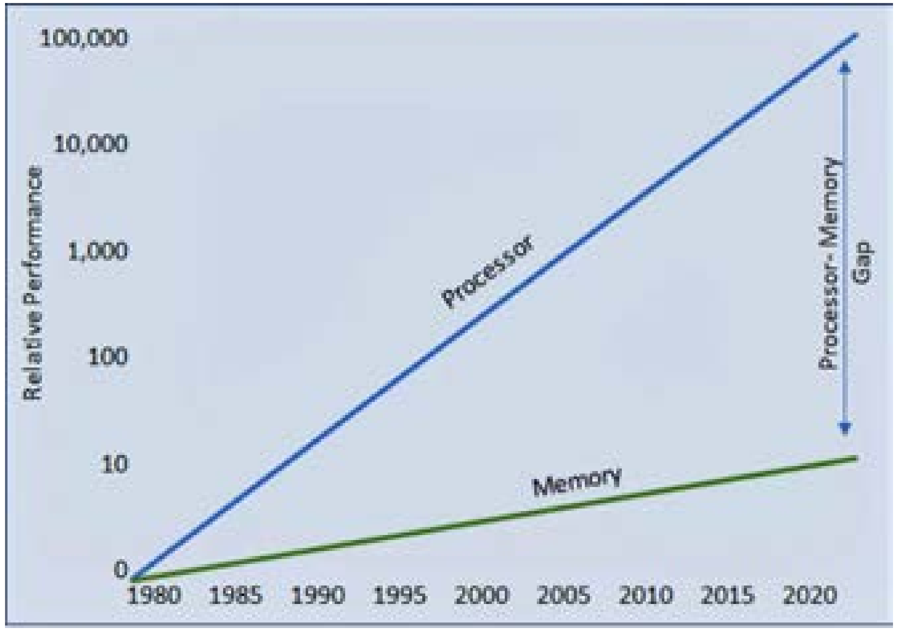
Advantages of multiferroic logic for edge computing solutions

- 100X lower switching energy than CMOS
- Potentially robust in extreme environments (radiation, temperature, …)
- Memory in logic for free (no memory wall problem)
    - 100x lower energy for memory access

➢ GPU without co-packaged optics and dense memory unit --> reduce system-level power consumption by 3400x

➢ >1200x reduction in power consumption --> Edge computing on a drone network or small satellite or F1 car for agile autonomous inference at the edge

Memory "wall:" system performance limited by memory access



Transition to American industry: foundry and system leaders such as Intel, AMD, TI, Analog Devices, Broadcom

Solving multiferroic interface challenges opens up opportunities in RF filters, Inertial sensors, Quantum MEMS.

Decoding Multiferroics' success will empower our warfighters with a technologically superior, foundational microelectronics capability

CMOS: Complementary Metal-Oxide-Semiconductor
GPU: Graphics Processing Unit
RF: radio frequency
MEMS: micro-electro-mechanical systems

Important Dates

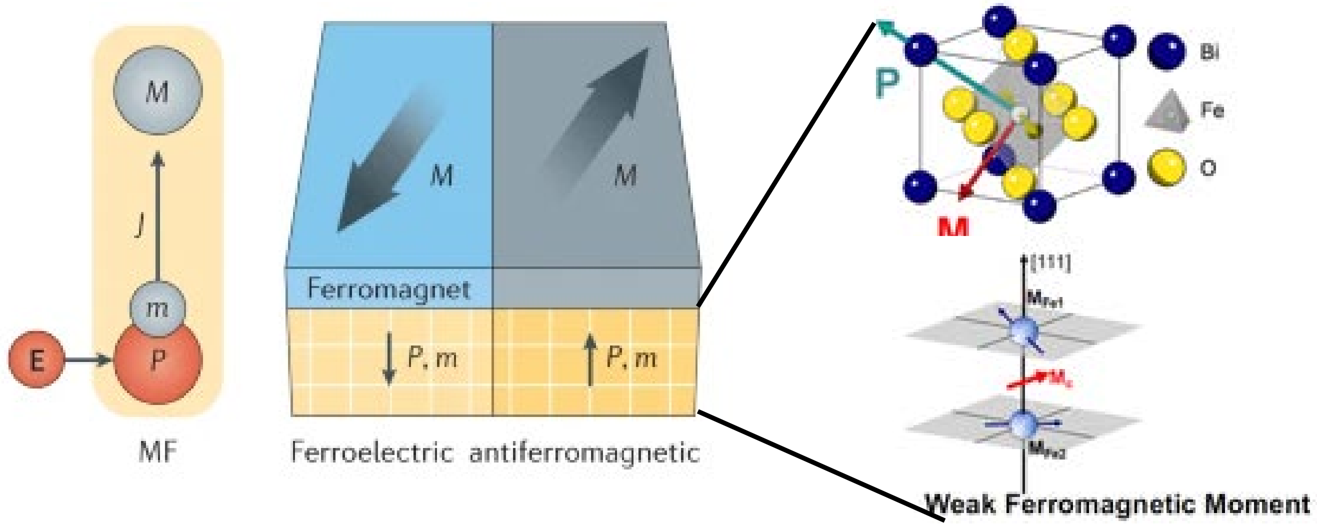
- DO Posted (DARPA-PA-25-07-01): January 30, 2026
- Proposer Profiles: February 6, 2026, at 4:00pm ET
  - Interested in collaboration opportunities send your contact information, a brief description of your technical competencies, and, if applicable, your desired expertise from other teams/organizations to fastandcurious@darpa.mil
- Abstracts Due: February 19, 2026, at 4:00pm ET
- Full Proposals Due: March 31, 2026, at 4:00pm ET
- Program Start: ~June 1, 2026

Information in the published DO supersedes material in this briefing.

www.darpa.mil

Deep Dive: Switching time delay

Current approach in ME logic: spin mediated multiferroic coupling



Magnetoelectric coupling in composite multiferroic heterostructures

Coupling mechanism	Materials	Converse ME coupling α_E (ultra thin films)
Self-assembled	CFO/BTO	1×10^{-8}
Spin-mediated	CoFe/BFO	1×10^{-7}
Strain-mediated	FeGaB/PZN-PT	3×10^{-7}
Goal		$>1\times10^{-5}$

- Fundamental limit of ferroelectric switching allows for picosecond switching time (elastic dynamics)
- For magnetoelectric multiferroics, the switching time is limited by magnetization switching time τ_m
- Depends on the *effective magnetic field* seen by the magnet via the magnetoelectric coupling α_E

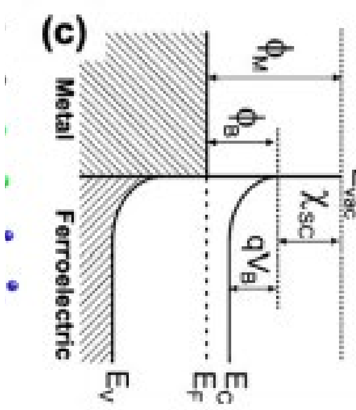
$$\tau_m \sim \frac{1}{\gamma H_E}, \qquad H_E = \alpha_E E, \qquad \alpha_E = \mu_0 \frac{dM}{dE}$$

- Strongest couplings are *two orders magnitude away*
- Spin-based multiferroic coupling is too weak to achieve switching time because the interaction is based on slight canting of antiferromagnet lattice

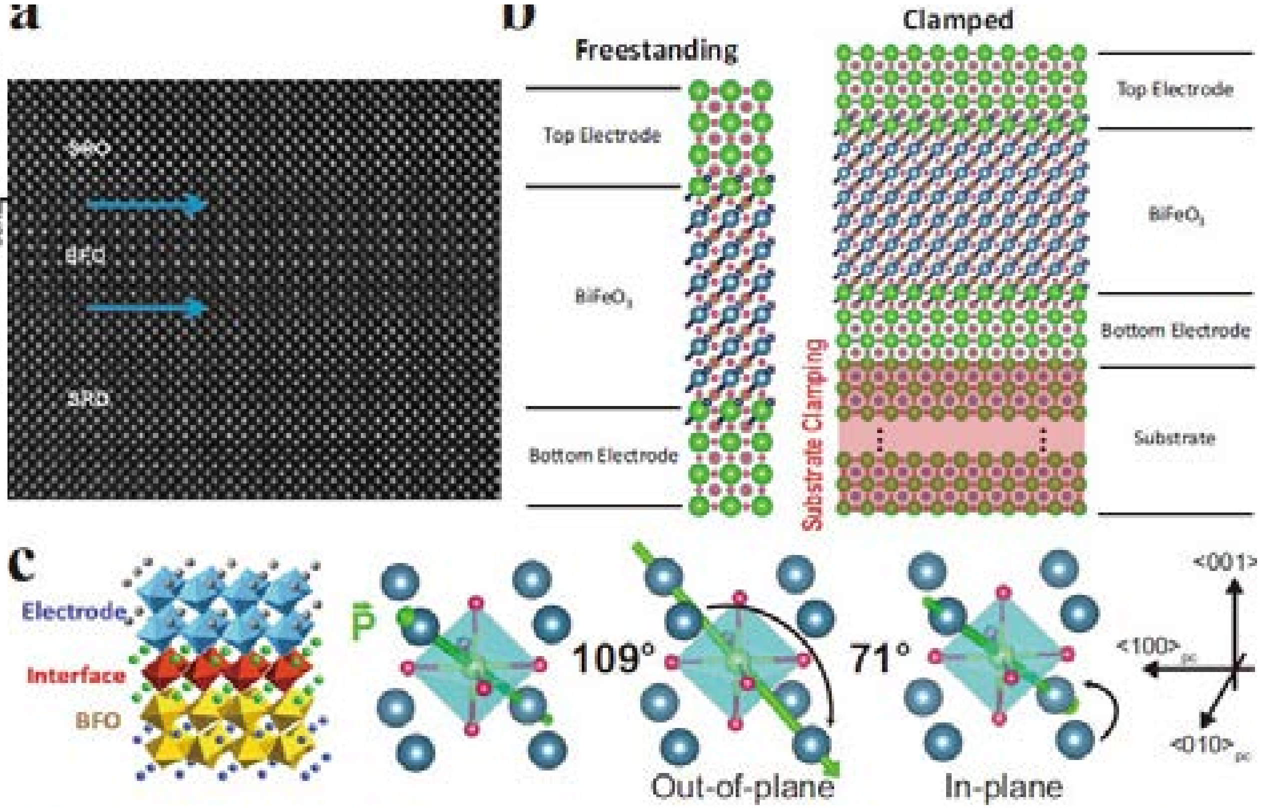
ME: magnetoeletric

Figure from Fiebig, Manfred, et al. Nature Reviews Materials, 2016

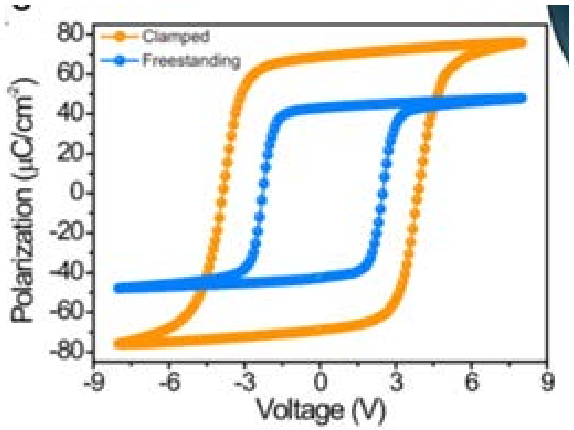
Deep Dive: Clamping Loss



Schottky barrier



40% reduction of the switching voltage through de-clamping



- Strain and tilt engineering: clamping vs free standing
- Lattice orientation, dynamics, and defects

B. Prasad et al.,. Adv. Mater., 2020
Fert, Albert, et al. RMP 2024