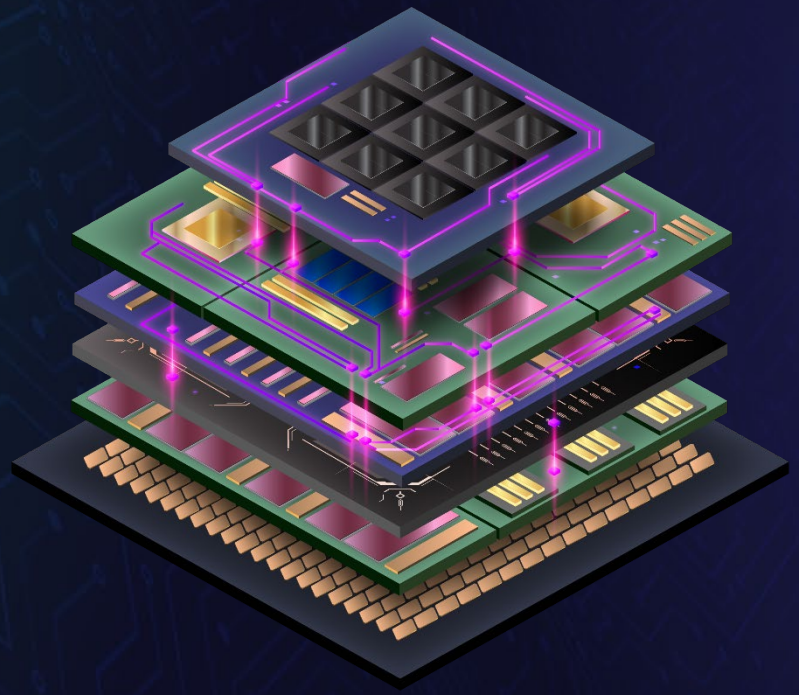
Next-Generation Microelectronics Manufacturing

NGMM Summit



TEXAS INSTITUTE FOR ELECTRONICS

The University of Texas at Austin

TNC Technology Roadmap Update

S.V. Sreenivasan

DARPA NGMM Summit

October 27, 2025

TOPICS

- Summary of Accomplishments To-Date

- Process Technology Roadmap:
  - Exemplar Microsystems as Drivers of Fab Capabilities
  - Planned 3DHI Fabrication Capabilities
  - Process Modules and Test Vehicles

- Concluding Remarks

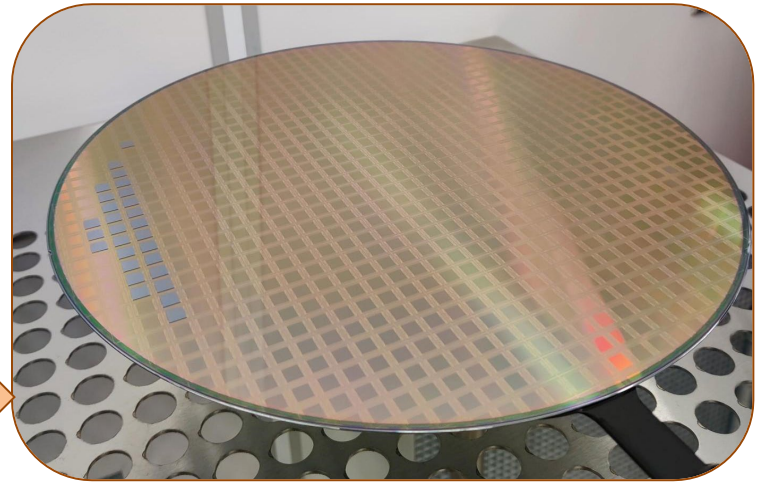
SUMMARY OF ACCOMPLISHMENTS TO-DATE

TIE Pickle Campus Fab: 18,000 SF Class 100 Cleanroom

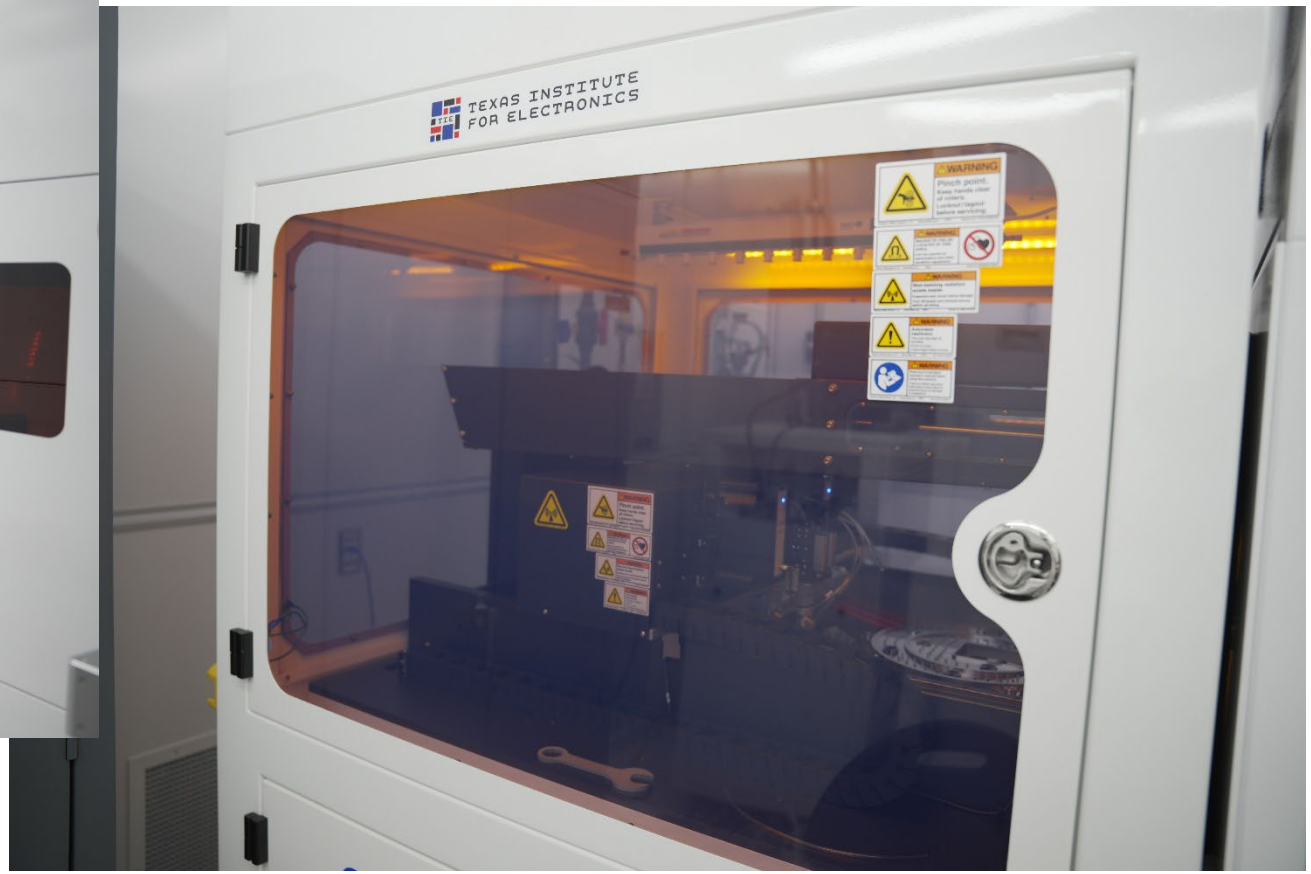
TIE Montopolis Campus Fab: 66,000 SF Class 100 Cleanroom

- Facility upgrades and equipment installation scheduled concurrently for efficient fab bring-up
- Cleanroom renovations and key equipment installation will be complete by January 2026.

- Established first process module (D2W hybrid bonding), obtained initial electrical yield, process optimization ongoing.



TIE Pickle Campus – Selected Equipment



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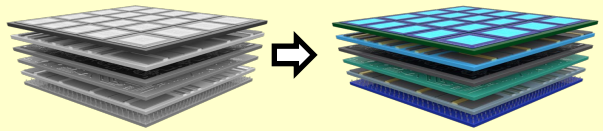
TNC PLANNED CAPABILITIES

TNC GOAL: DESIGN & FABRICATION OF MIXED-MATERIALS 3DHI MICROSYSTEMS BUILT ON 3D SI BASELINE
(SI, GLASS, GAN, INP, GAAS, SIC, FERRITE, HGCDTE)



3D SILICON BASELINE MIXED-MATERIAL 3DHI

PLANNED LVHM 3DHI TECHNOLOGY AND FOUNDRY PRODUCTS

1. Bonding

Die-To-Wafer	Die-To-Wafer & Wafer-to-Wafer
Thermocompression *Cu-Cu Cu-Sn*	Hybrid *Cu-Cu*

2. Through Substrate Via (TSV) and Advanced Substrates

Silicon	Glass
Compound Semiconductor	Polymer

Advanced Substrates

3. Routing and Reconstitution

Cu Routing Layers (200mm/300mm)
Cu Damascene, RDL/Bump

Sub-200mm Wafer Processing Enabled by Reconstitution

Mixed-material Reconstitution

4. Thermal Solutions for Mixed-material 3DHI

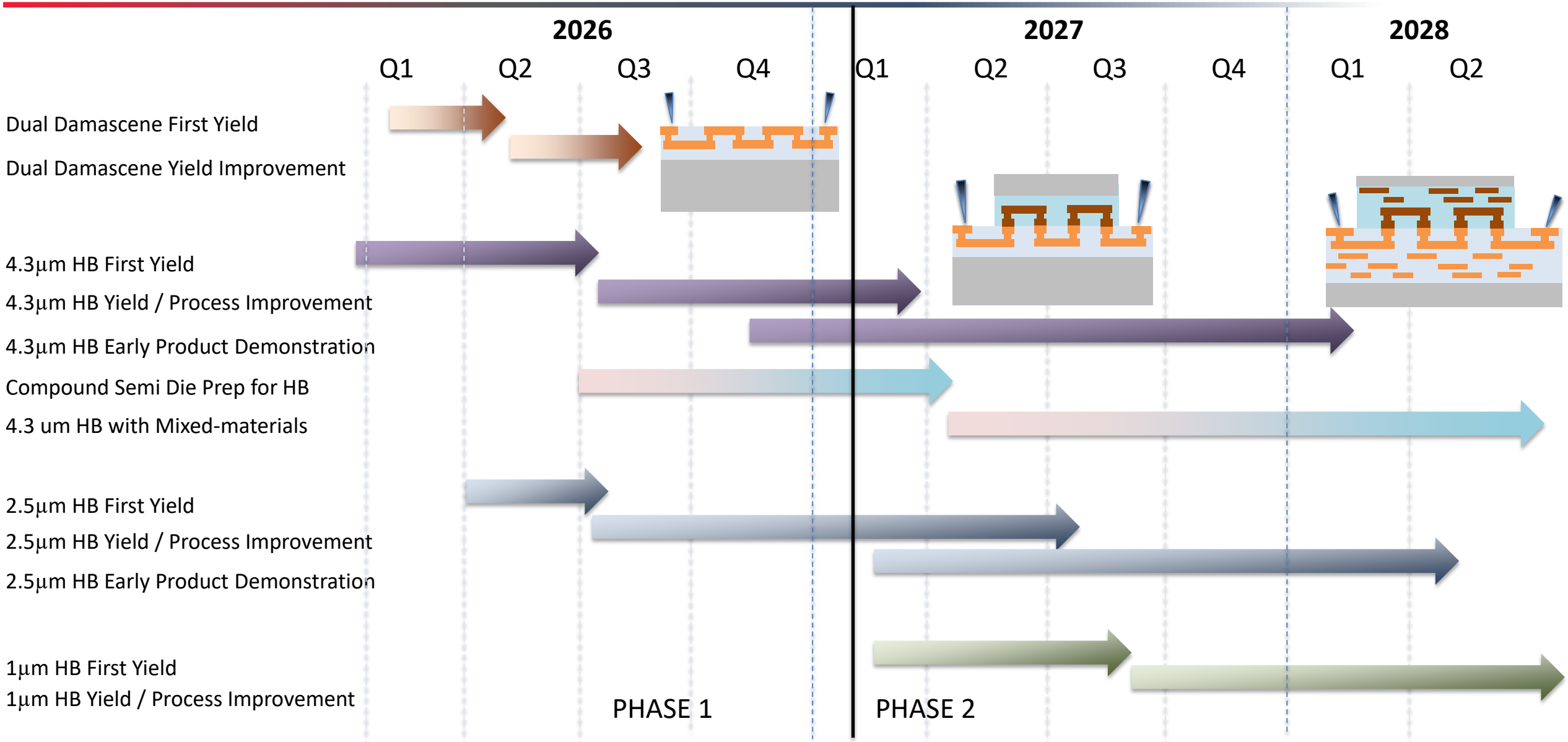
Engineered Thermal Materials & Systems

Thermo-mechanical Modeling & Reliability

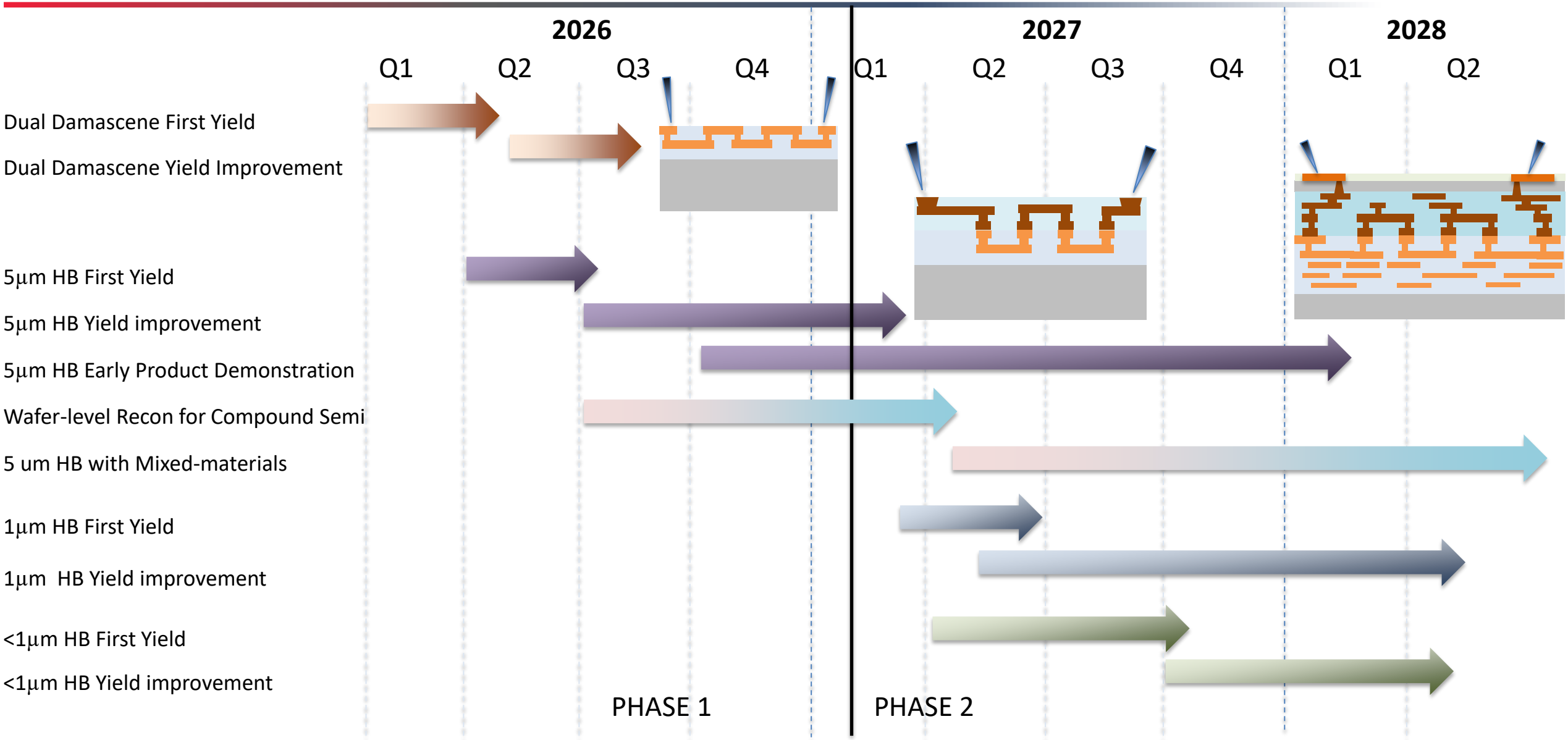
5. Failure Analysis, Characterization, Test & Reliability

6. EDA and 3D Assembly Development Kit (3D-ADK)

TNC D2W HB Roadmap



TNC W2W HB Roadmap



TNC TSV ROADMAP

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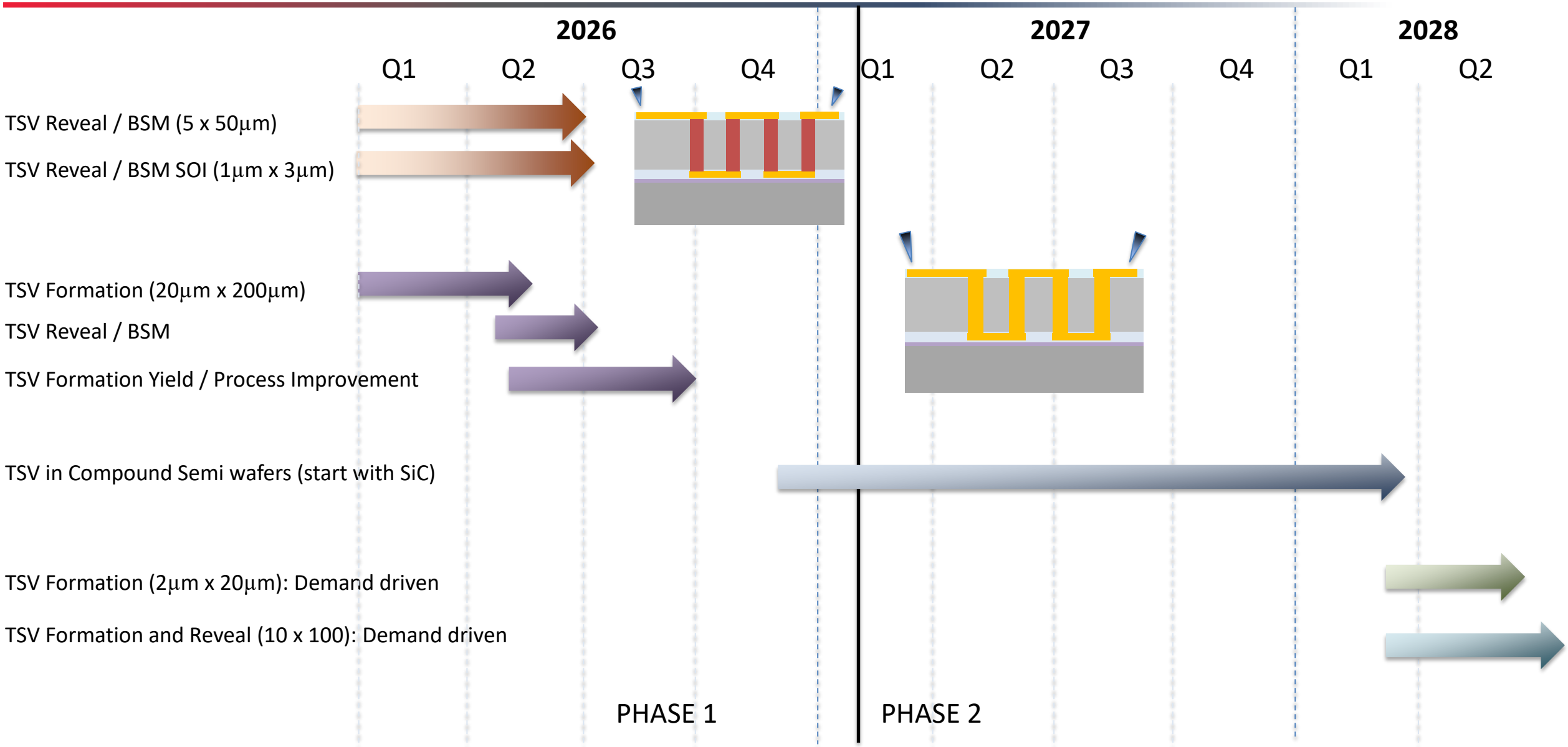
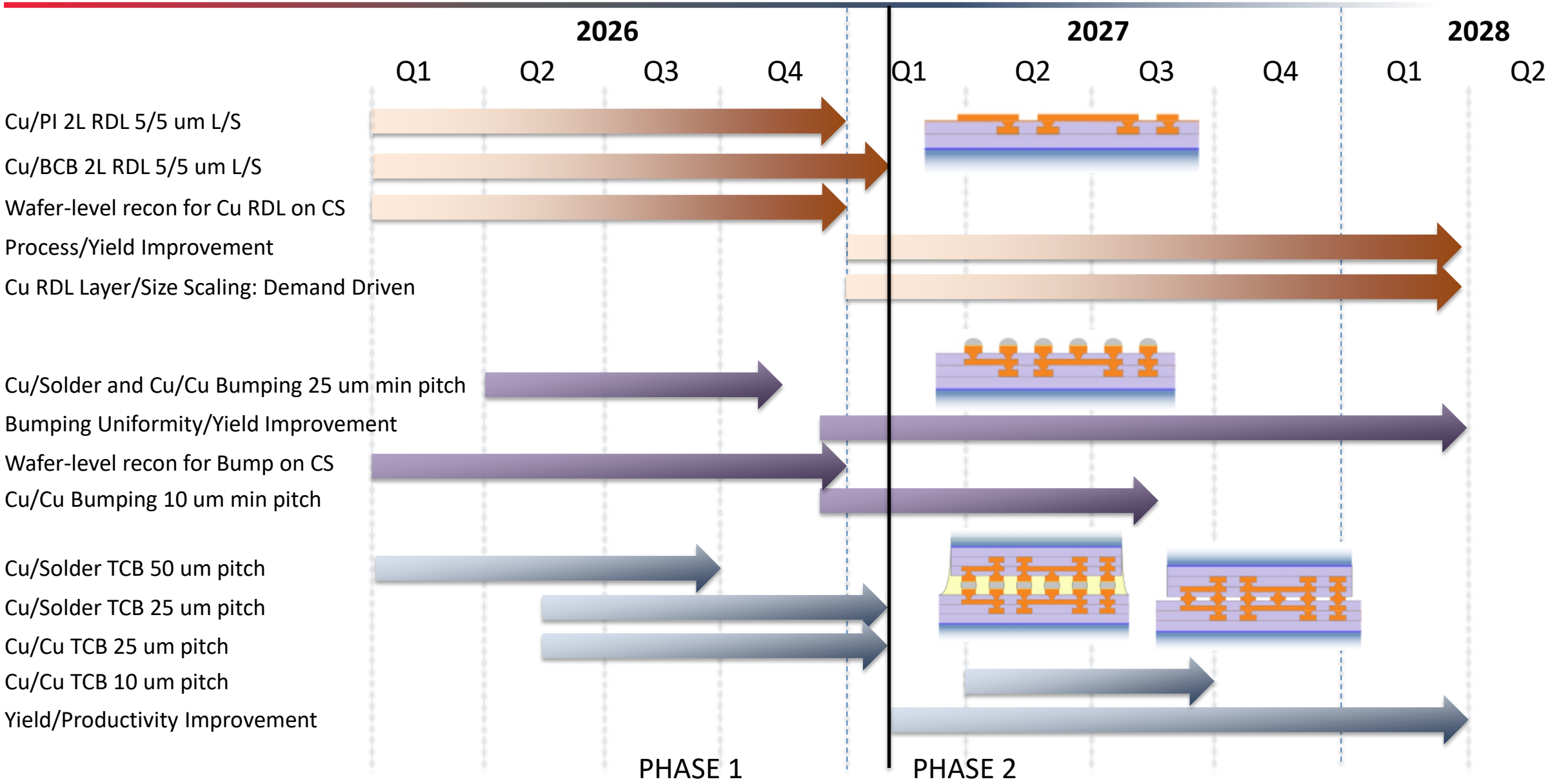


TNC RDL/BUMP/TCB ROADMAP



PI = Polyimide BCB = Benzocyclobutene

TIE NGMM Thermal Program

Thermal Strategy

Goal: Establish a mixed-material 3DHI thermal program by leveraging NGMM partnerships with materials/equip. suppliers, EDA companies, customers and universities.

Focus Areas:

- **Advance Package Thermals** (Active & Passive Cooling)
- **Optimize Process Thermals** (mixed-material 3DHI Assembly)

Program Impact:

- **Risk Mitigation**: Address thermal and mechanical challenges across the entire 3DHI stack (device to package).
- **Enable Transition**: Bring technologies into test vehicles and deploy as part of TIE ADK.

Thermal Plans

Intra-Stack Thermals:

- Integrate high thermal conductivity materials into the 3D stack.
- Develop active microfluidic cooling to address design/reliability challenges with various working fluids and wetted materials.

Intra-Package:

- Deploy multi-level heat spreading technologies through an experimental / modeling design-aware optimization approach.
- Expand partnership with major EDA vendors for mixed-material microsystems.

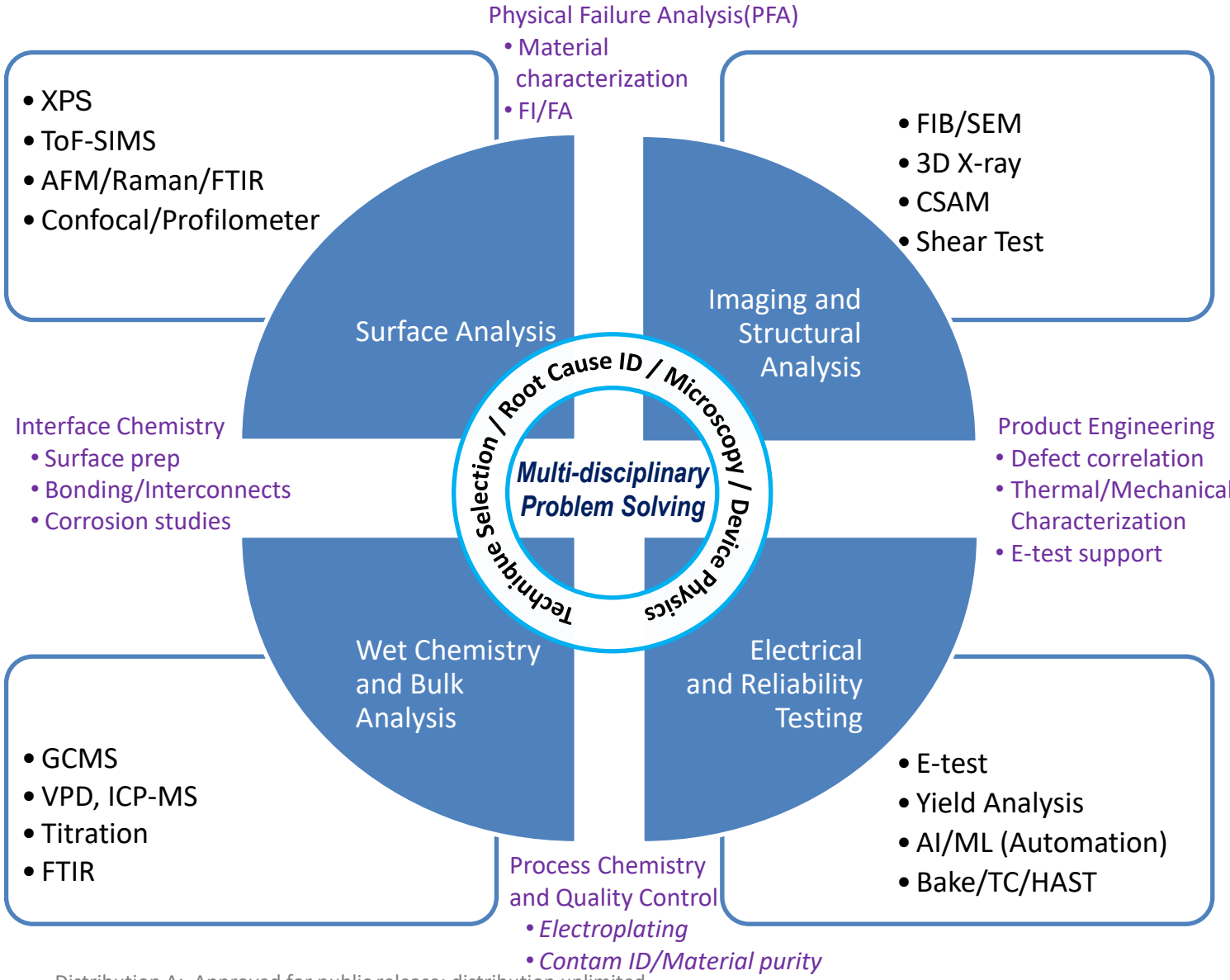
Process & Metrology:

- Address thermal-mechanical challenges in 3DHI assembly (e.g., CTE mismatch in mixed material systems).
- Develop sub-surface, full-field thermal measurement techniques coupled with novel embedded test structures.

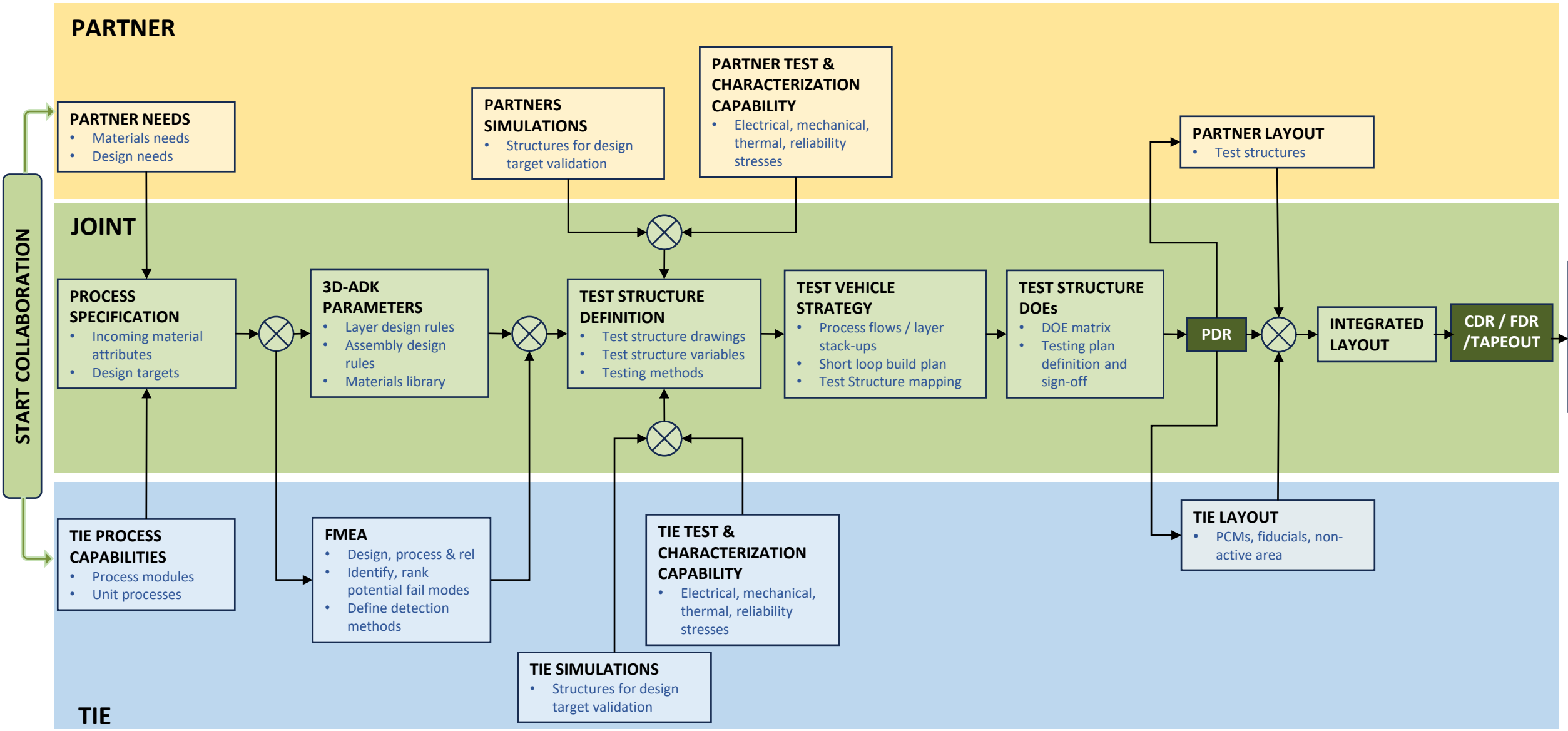
FAILURE ANALYSIS, CHARACTERIZATION & TEST LABS

Lab Mission: Establish center of excellence for failure analysis, fault isolation, process optimization, close partnerships with equipment/material suppliers and enabling end customers.

Lab Personnel: Engineers, scientists and technicians with significant R&D and industry experience in lab infrastructure for advanced package failure analysis and characterization.



TEST VEHICLE DESIGN PARTNERSHIPS



CURRENT PROGRAM TEST VEHICLES METRICS

	CURRENT PROGRAM TEST VEHICLES			
Physical interfaces	**Ka and W Band RF PA TVs**	**Digital TVs**	**IR FPA TVs**	**Power Convertor TVs**
Hybrid bond pitch	**N/A**	**2.5 µm**	**5 µm**	**N/A**
Bump pitch	**50 µm**	**25 µm**	**10 µm**	**20 µm**
Number of integrated 2D chips	**3**	**2**	**3**	**4-5**
Number of base materials	**3**	**1**	**2**	**2**
Digital interfaces				
Energy efficiency		**0.01 pJ/bit**		
Latency		**TBD**		
Areal bandwidth density		**3125 GBps/mm^2**		
Analog interfaces				
Center frequency	**Ka-band**			**MHz**
3 dB bandwidth	**18 – 50 GHz**			
Insertion loss	**0.26 dB**			

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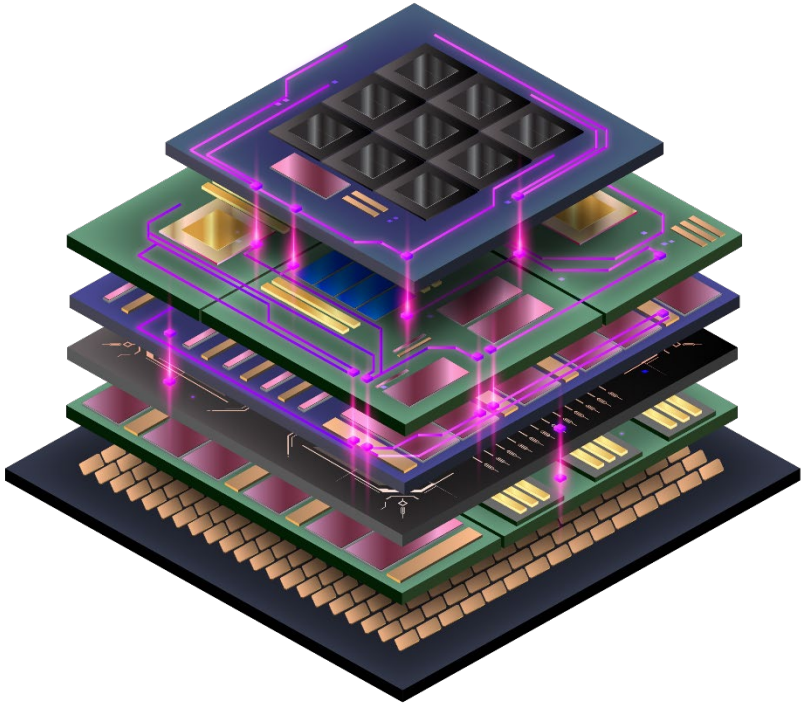
CONCLUDING REMARKS

- Facilities nearly complete at Pickle and Montopolis Fabs
- Equipment installation ongoing
- Current test vehicles include RFPAs, Digital, IR-FPAs and Power Convertors
- Establishing collaborative approach for creating test vehicle roadmap with partners

THANK YOU



For more information, visit:
TXIE.ORG