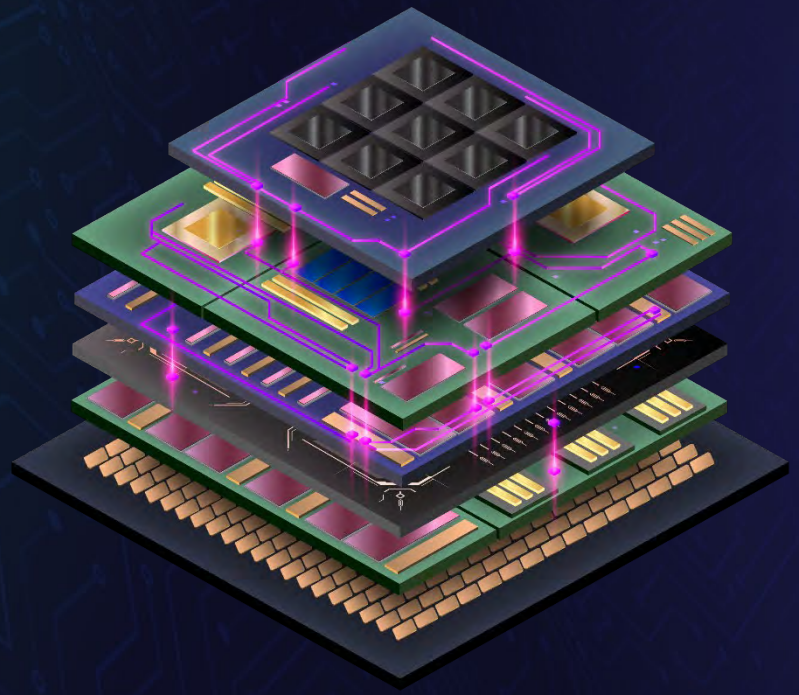
Next-Generation Microelectronics Manufacturing

NGMM Summit



TEXAS INSTITUTE FOR ELECTRONICS

The University of Texas at Austin

TIE NGMM Center Overview

Dwayne LaBrake

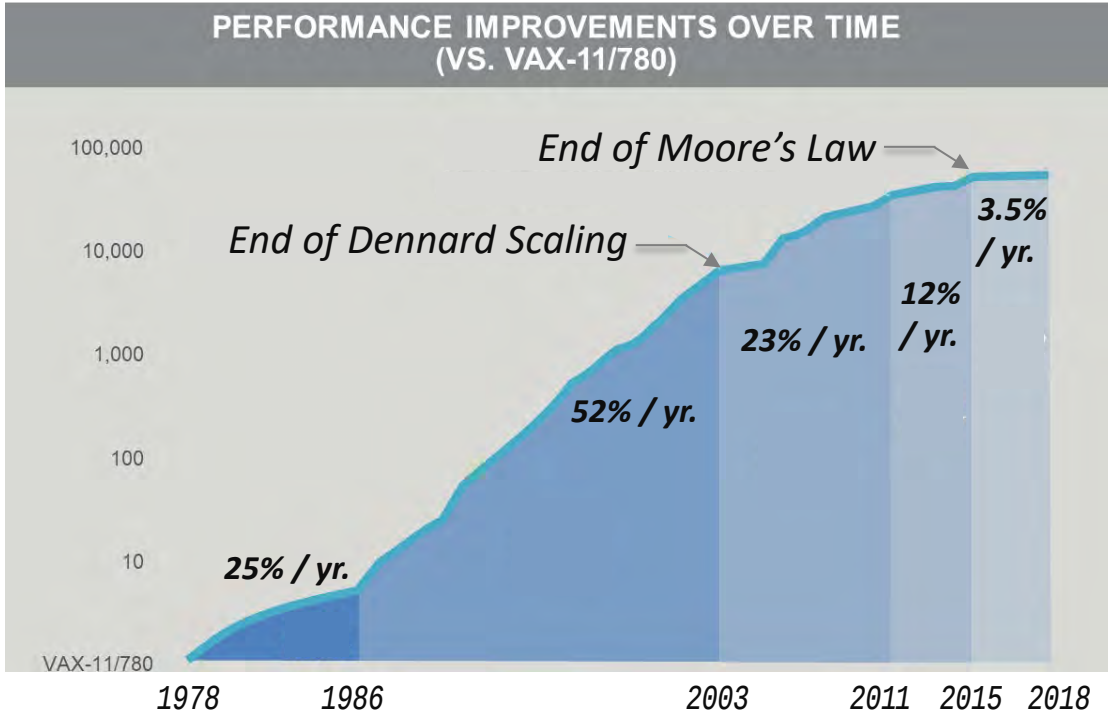
DARPA NGMM Summit

October 27, 2025

Contents

- Semiconductor Industry Trends
- Introduction to TIE
- DARPA NGMM Program at TIE
- NGMM Program Business Model
- Summary and Q&A

Slowing of Moore's Law (2D Scaling), Need for 3DHI



John Hennessy and David Patterson, Computer Architecture: A Quantitative Approach, 6/e. 2018

TSMC Predicts 1 Trillion Transistor GPU by 2034 with 3D Integration

"…typical [~100 billion transistor] GPU chips used for AI training have already reached the reticle field limit. …increasing transistor count will require multiple chips, ***interconnected with 2.5D or 3D integration****… We forecast that within a decade a* ***multichiplet GPU*** *will have more than 1 trillion transistors.* ***We'll need to link all these chiplets together in a 3D stack.****"*

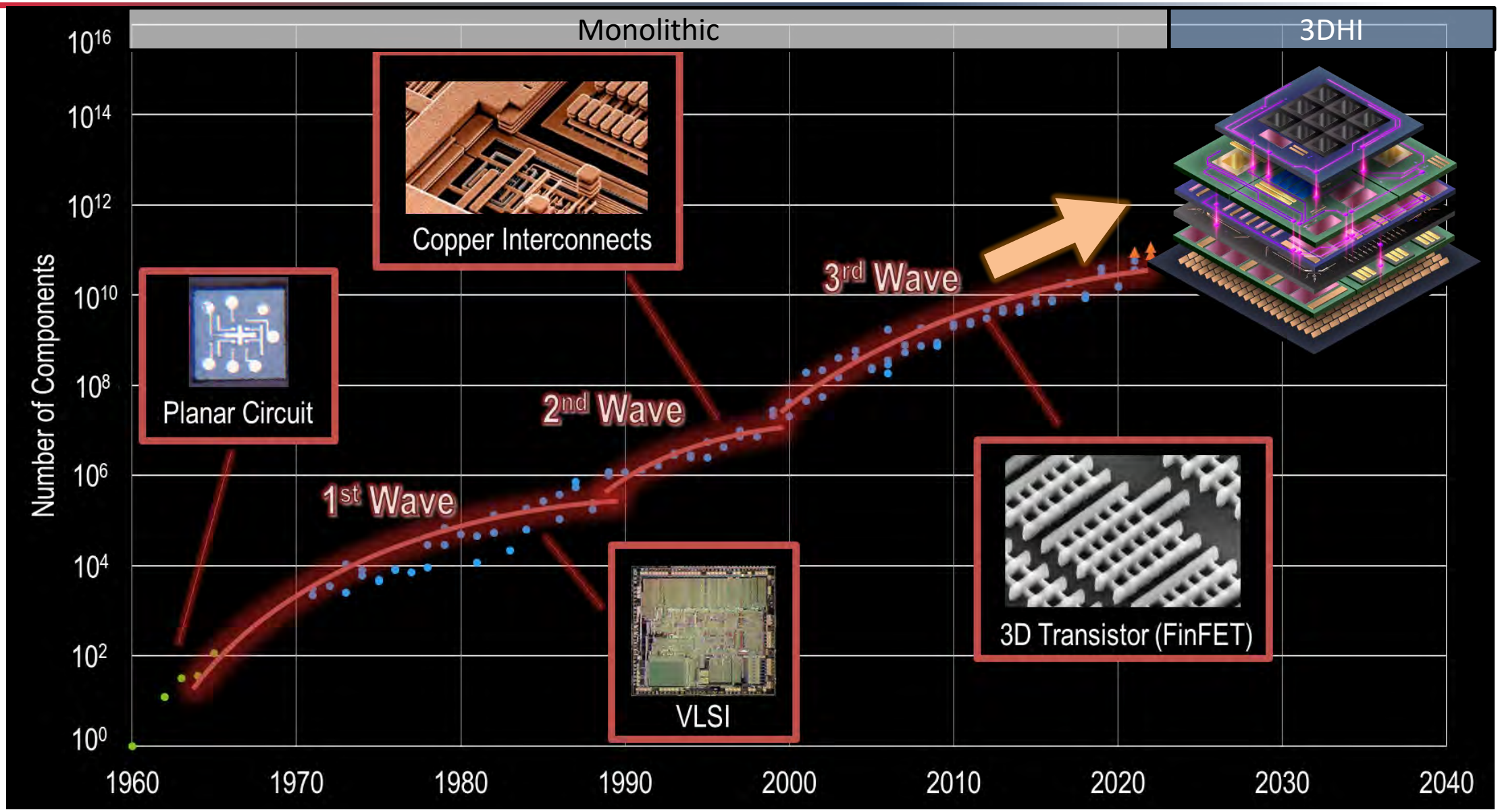
https://spectrum.ieee.org/trillion-transistor-gpu/toward-a-trillion-transistors

ASML Statement on Advanced Packaging

ASML states that "*as the pace of 2D shrink slows, chipmakers are relying more and more on exotic materials,* ***advanced packaging technologies*** *and more complex 3D transistor designs to deliver improved chip performance*."

https://www.asml.com/en/technology/all-about-microchips/moores-law

Semiconductor Technology Roadmap Evolution

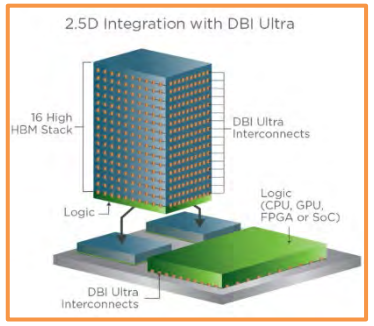


Aggressive Pitch Scaling is the key

3D Si for Flash Memory

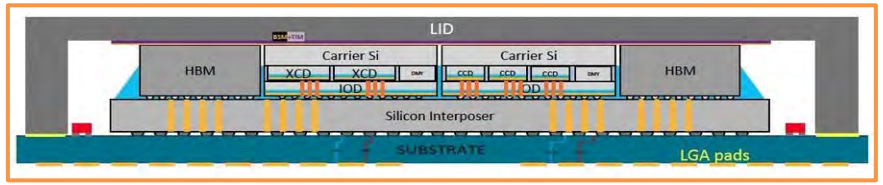
World's First 176-Layer NAND Achieves Breakthrough Performance and Density
By Gary Hilson, 11/16/2020, EE Times

Stacked DRAM*



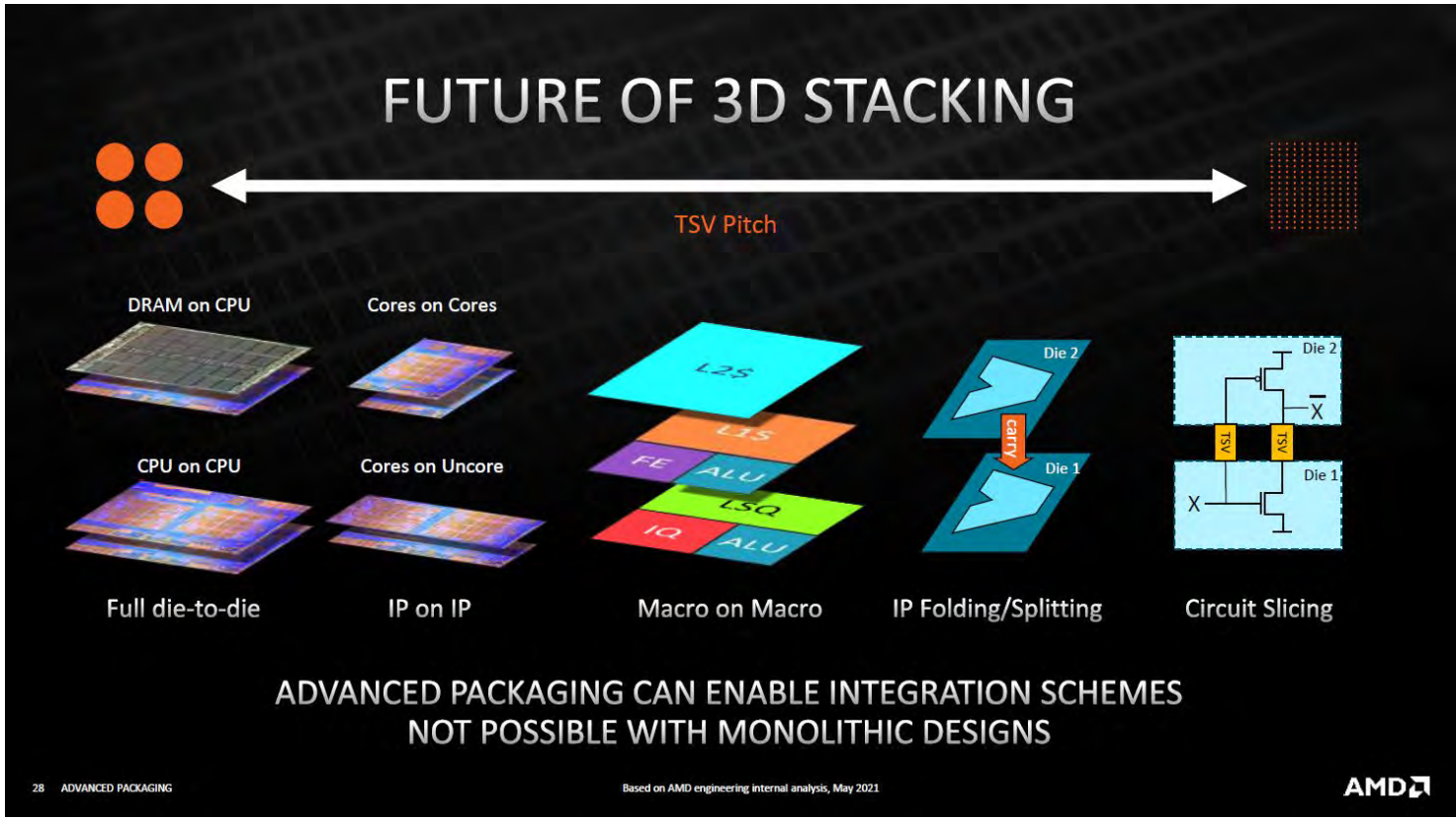
Device disaggregation coupled with hybrid bonding pitch reduction is the new horizon for device performance improvement

AMD MI300 GPU



"AMD's Next GPU Is a 3D-Integrated Superchip"
By Samuel K. Moore, IEEE Spectrum, December 6th, 2023

AMD Roadmap for 3D stacking

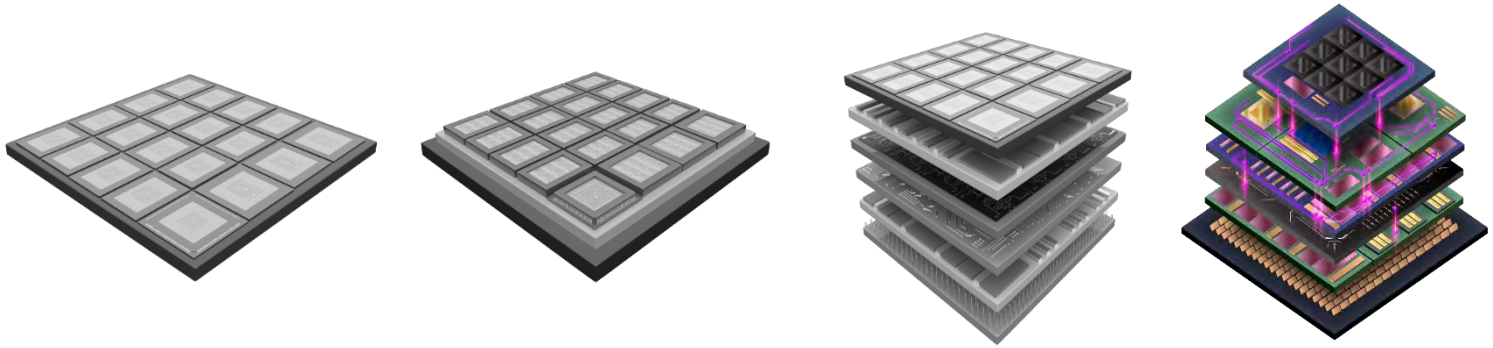


**Hybrid Bonding for the Next Generation of High-Performance Devices*
Laura Mirkarimi, Nov 2023
IMAP Source Proceedings 2022 (DPC)

"The next frontier: Enabling Moore's Law using heterogeneous integration"
By Raja Swaminathan
Chip Scale Review, Volume 26, No. 3, May/June, 2022, Page 18

2D Moore's Law to Multi-Material 3DHI

2D → 2.5D → 3D → 3DHI

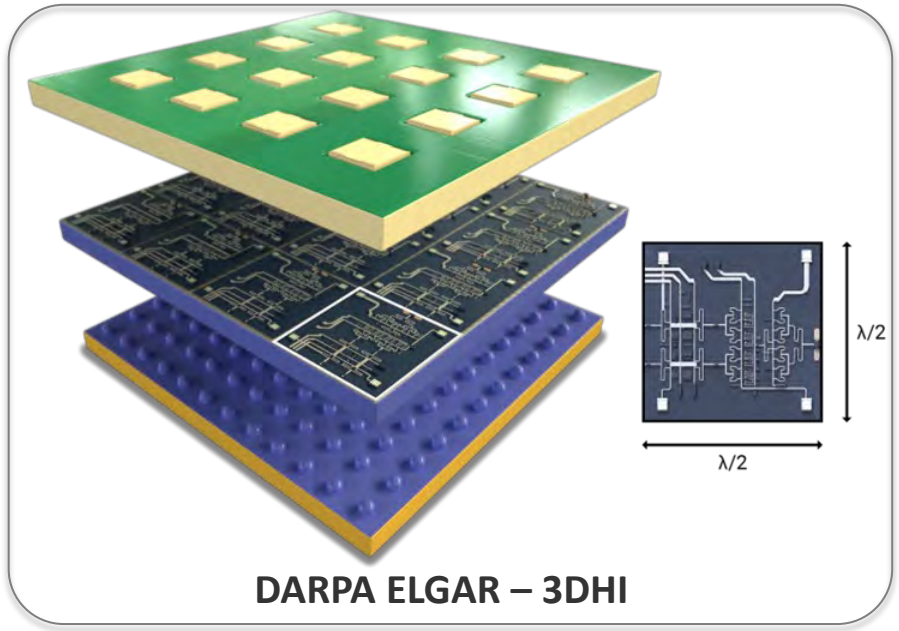


Silicon → NGMM Mixed Materials

Performance

1x → 3x → 30x → 100x

DARPA



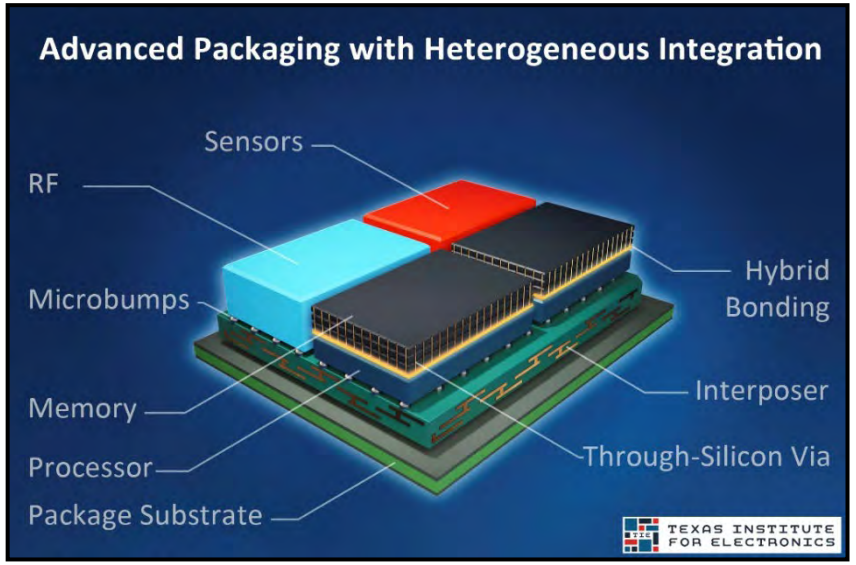
DARPA ELGAR – 3DHI

Changes in US Advanced Packaging Ecosystem

US Department of Defense and IPC

National need for a domestic, non-profit, open-access 3DHI fab facility that supports:

- Fabrication of advanced multi-material 3D microsystems
- Rapid innovation through 3DHI R&D and prototyping
- Pilot manufacturing
- ITAR/EAR compliant operations and IP security
- Efficient low-volume, high-mix fabrication



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TIE Funding

TIE History:

- Founded in April 2021 to address advanced heterogeneous integration and packaging in the U.S.
  - **Founders**: SV Sreenivasan, Paras Ajay, Shrawan Singhal, and Larry Dunn
- Grew out of the Nanomanufacturing Systems Center (NASCENT), an Engineering Center funded by **NSF** for semiconductor manufacturing.

2022 TIE First Funding

- $112M: State of Texas

2023 Texas CHIPS Act

- $440M: Construction

2024 DARPA NGMM Award

- $840M: 3DHI Foundry

2025 Texas Semiconductor Innovation Fund Award

- $54M: Construction

TIE is leveraging two UT-Austin campuses with commercial-grade fabs and Texas state funds to build state-of-the-art 3DHI process capabilities.

TIE Leadership Team

Senior Executives

Dwayne LaBrake, TIE CEO
Board Member

S.V. Sreenivasan, TIE Founder/CTO,
Board Member

Dave Gino
TIE CFO

Tom Weichel
SVP of Operations

Srikanth Gondi, Executive
Director Business Strategy

Department Heads

Sharath Hosali, Director
Process Integration

Leonel Arana, Executive Director
Manufacturing Integration

Alyssa Reinhart, Director
Workforce Development

Shankar Devasenathipathy
Director Character/Failure

Pratik Joshi, Executive
Director Unit Process

Janet Monaco, Director
Administration

Executive Board Members

Will Inboden, UT Provost
Board Member

Meghali Chopra
Board Member

Ken Joyce
Board Member

Major General (Ret.) Jeannie
Leavitt, Board Member

Babak Sabi
Board Member

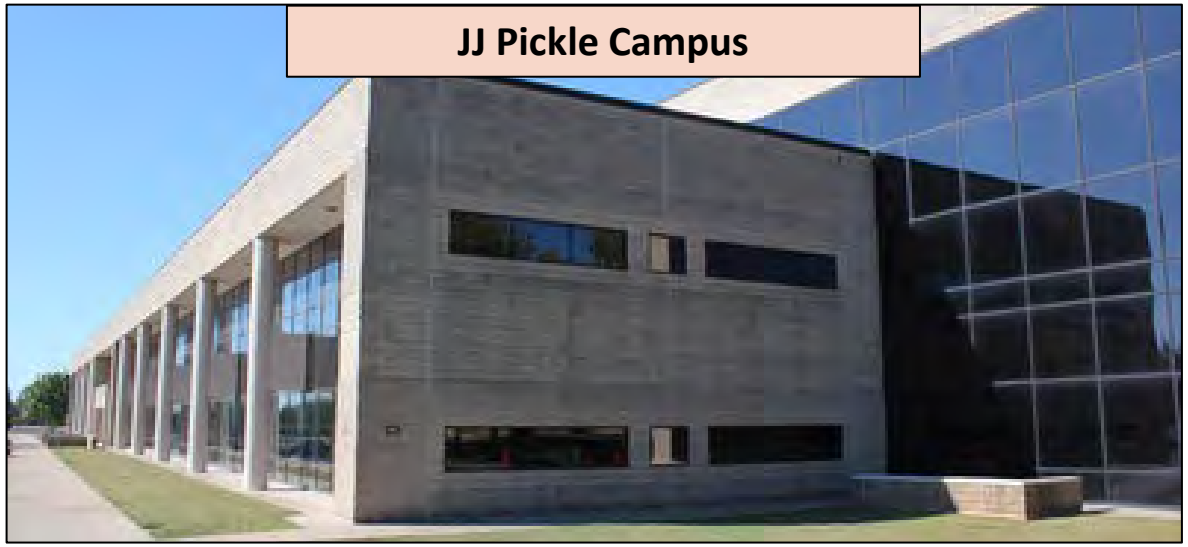
John Schreck
Board Member

Michael Holmes, NGMM Managing
Director, Board Member

TIE Fab Facilities

Montopolis Campus

JJ Pickle Campus



TIE NGMM Center (TNC) will be a 3DHI Low Volume High Mix (LVHM) foundry with SOTA equipment, process/design enablement, including DIBs, equipment and EDA companies, foundries, startups and universities.

Two campuses with fabs, approximately 15 minutes apart	

• Class 100 cleanroom space for 3DHI: 84,000 square feet
  • Montopolis (LVHM foundry): 66,000 square feet
  • Pickle (R&D Fab): 18,000 square feet
	• Office space: more than 220,000 square feet
	• 100+ acres for collocated future expansion
	• Can add Class 1000 cleanroom space as needed

CONTENTS

In July 2024, UT Austin was awarded $840M for DARPA's Next Generation Microelectronics Manufacturing (NGMM) program. The DARPA award leverages an additional $606M state of Texas investment in TIE.

Texas CHIPS Act

NGMM Program Goals Toward Commercial Sustainability:

Advanced Technology Roadmap for 3DHI Manufacturing

De-risk unit process, process module and metrology technologies

Low-volume, High-mix (LVHM) Mfg. Fab. for 3DHI Microsystems

Establish a foundry for LVHM manufacturing for defense and commercial sectors

Electronic Design Automation Support

TIE's design support group is the "store front" for customers using the Foundry

Comprehensive Workforce Development Program

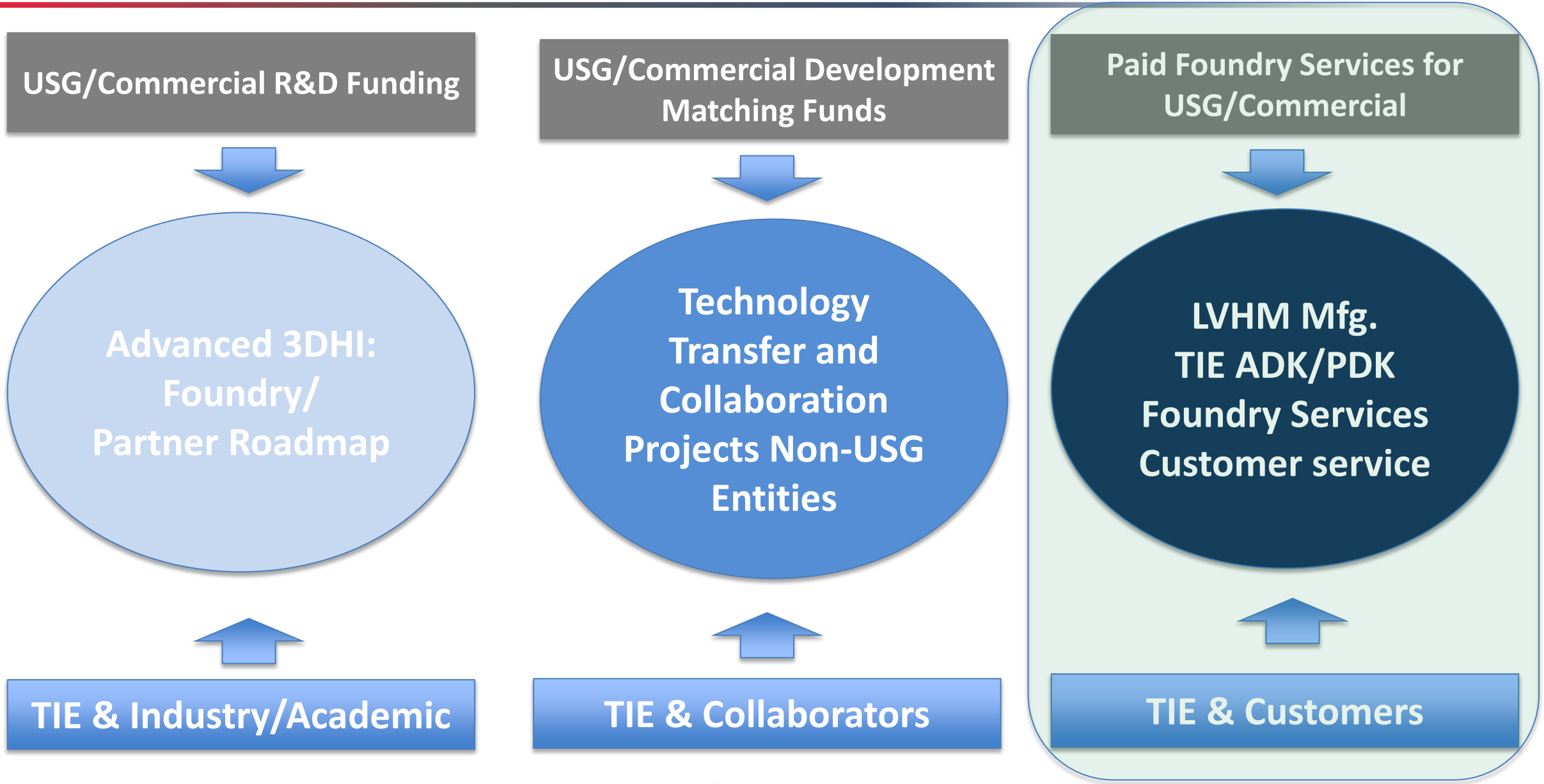
Establish a premier comprehensive semiconductor workforce development in 3DHI, and share best practices nationally

PLANNED LVHM 3DHI TECHNOLOGY AND FOUNDRY PRODUCTS

1. Bonding (Chip Stacking)
2. Through Substrate Via (TSV) and Advanced Substrates
3. Routing and Reconstitution
4. Thermal Solutions for Mixed-Material 3DHI
5. Failure Analysis, Characterization, Test and Reliability
6. EDA and 3D Assembly Development Kit (3D-ADK)

All process lines enabled using manufacturing execution system (MES)

NGMM Access Funding Models



NGMM Program Plan Summary

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Phase 1
Establish Baseline Process

Phase 1 Deliverables
1. Initial Process Capability
2. Alpha ADK

Phase 2
Qualify / Operationalize

Phase 2 Deliverables
1. Qualified Process Capability
2. Beta ADK

End Goal
Ready for Customers

- **Facility Preparation and Equipment Installation**
  - Facility Refurbishment
  - Equipment Procurement and Installation
- **Process Development**
  - Initial Process Capability Development
- **Electronic Design Automation**
  - Workflows and Simulation
  - 3D-Assembly Design Kit (ADK)

- **3DHI Prototyping**
  - Exemplar Microsystems and Design Challenge Prototypes to Exercise Process Capability
- **Process Improvement**
  - Automation of Fabrication, Assembly, and Test Processes
- **Emulation/Digital Twin Capability Development**

- **3DHI Capability**
  - ✓ **High Performance HI Microsystems**
  - ✓ **Research, Rapid Prototyping, and Manufacturing**
  - ✓ **Foundry Services**
  - ✓ **ITAR/EAR Compliant**
  - ✓ **Self-Sustaining**
  - ✓ **Cost Effective**

Phase 1: 30 months | **Phase 2: 30 months** | **3DHI Foundry Capability**

Today

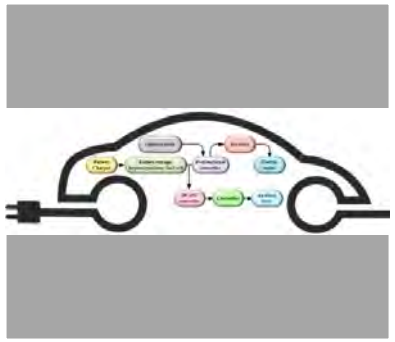
July 2024 | Oct 2025 | Jan 2027 | Feb 2027 | May 2028 | July 2029

NGMM 3DHI Exemplars (Dual Use)

freepik.com

onsemi.com

UT Austin



Electronics 2022, 11(4), 562

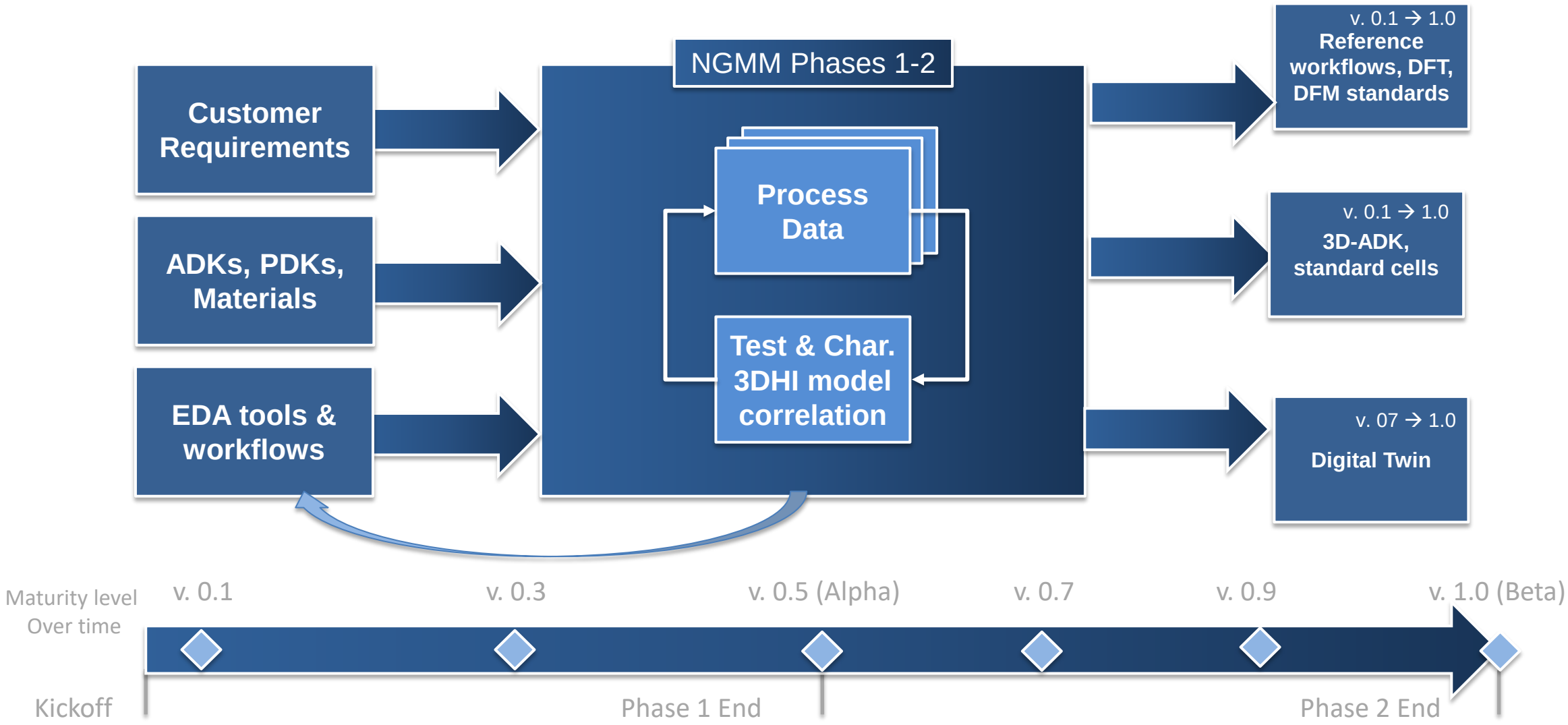
Boeing

1. Phased Array	2. Focal Plane Array	3. Compact Power Converter
5G/6G Communications	Intelligence, Surveillance, Reconnaissance	Satellites/Spacecraft
Satellite Communications	Missile Warning and Tracking Missions	Air Vehicles
Software Defined Radio	Sensors for Advanced Infrared Search and Tracking Systems	Radiation Hardened Electronics
Weapons Detection	Environmental Monitoring	Electric Vehicles
Sensing in Degraded Visual Environments	Sensors for Autonomous Vehicles	Missile Seekers
High Bandwidth Communications	Sensors for Robotics	High Efficiency Computing Systems
Radar for Automotive, Air and Missile Defense, Ground Surveillance		On-Chip Power Conversion

Edge Compute

Exemplars Drive NGMM Technology Roadmap and Enable a Broad Range of DoW and Commercial Applications

EDA / 3D-ADK Design and Test Workflow



Ecosystem Supporters

AMD, Applied Materials, ASU Southwest Advanced Prototyping Hub (Arizona State University), Benchmark Technology Group, Canon, DECA, intel, Micron, Raytheon An RTX Business, Resonac, Samsung, skywater, Tower Semiconductor

TEXAS INSTITUTE FOR ELECTRONICS

Academic Partners

Austin Community College District, Georgia Institute of Technology, PennState College of Engineering, Prairie View A&M University, Purdue University, Rice, Texas A&M University Engineering, Texas State University, Texas Tech University, UC San Diego, University of Houston, UNT University of North Texas, UTA The University of Texas at Arlington, Texas The University of Texas at Austin, UT Dallas, UTEP, The University of Texas Rio Grande Valley, UTSA The University of Texas at San Antonio

Industrial Sub-Awardees

Ansys, Applied Materials, BAE Systems, cadence, Boeing, electroninks, GlobalFoundries, HRL Laboratories, Lockheed Martin, micross, Northrop Grumman, qorvo, Raytheon An RTX Business, sandbox Semiconductor, Siemens Government Technologies, Synopsys, Teledyne Technologies Incorporated, 3DGS, zero

NGMM Workforce Development

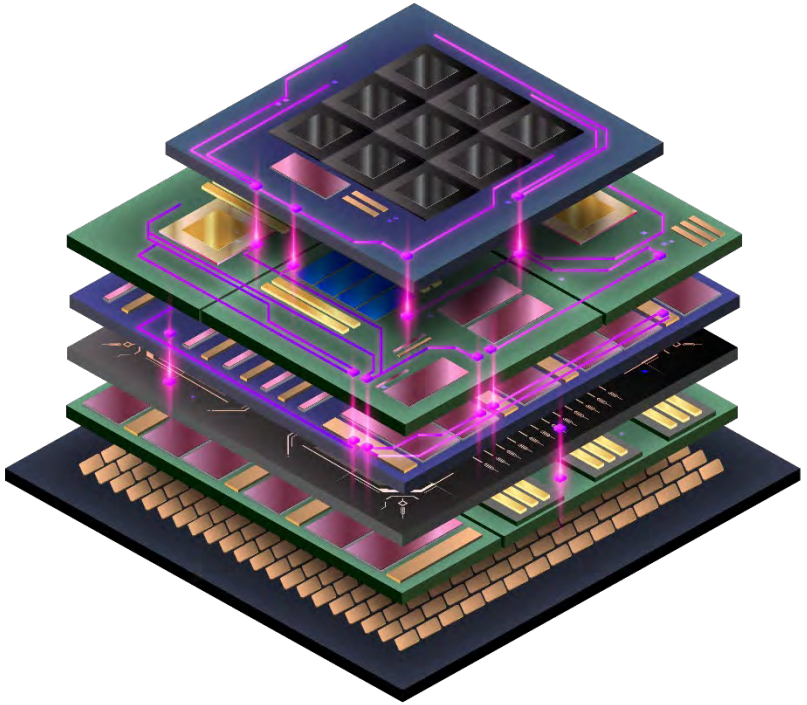
- Training center (approximately 25,000 square feet) next to NGMM 3DHI Foundry at Montopolis
- Joint initiative between ACC, UT Austin, and TIE
  - Broader support for the region and state
- Advanced Packaging Focused hands-on training in:
  - Equipment maintenance and repair
  - Packaging process technology
  - Metrology, data analytics
- TSIF funding to build training center

Summary

- **Semiconductor Industry Trends**
  - 2D Scaling to 3DHI is accelerating
  - Many of the key IDMs and Foundries announced advanced packaging facilities will be built in the US
- **TIE – Focused on 3DHI Manufacturing Technology and LVHM Manufacturing**
- **DARPA NGMM Program at TIE**
  - Program goals → Mixed material 3DHI technology roadmap, LVHM foundry, EDA capability and workforce development
  - ADK/PDK → Foundry access
  - Process modules, test vehicles in progress to feed ADK
  - Exemplar applications in RF Phased Arrays, Focal Plane Arrays, Power Convertors and AI Hardware
  - State of the art Foundry including MES and full test and reliability capabilities
  - Workforce development program in 3DHI – technician training, undergraduate minor and MS programs

VIDEO

THANK YOU



For more information, visit:
TXIE.ORG