Heterogeneous Integration in Analog Technologies

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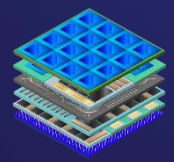
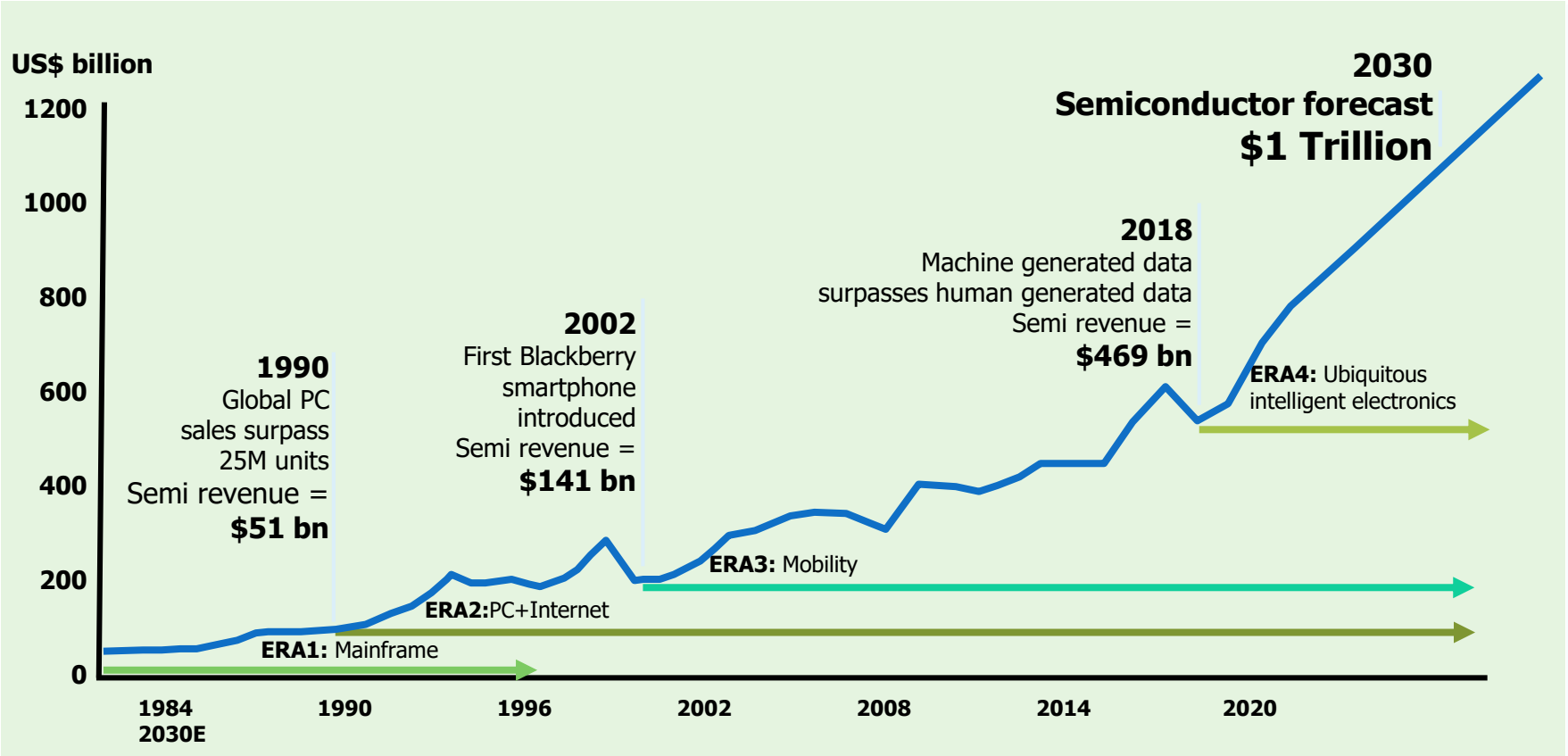
NGMM Summit
2025



Market growth | driven by technology disruptions and trends

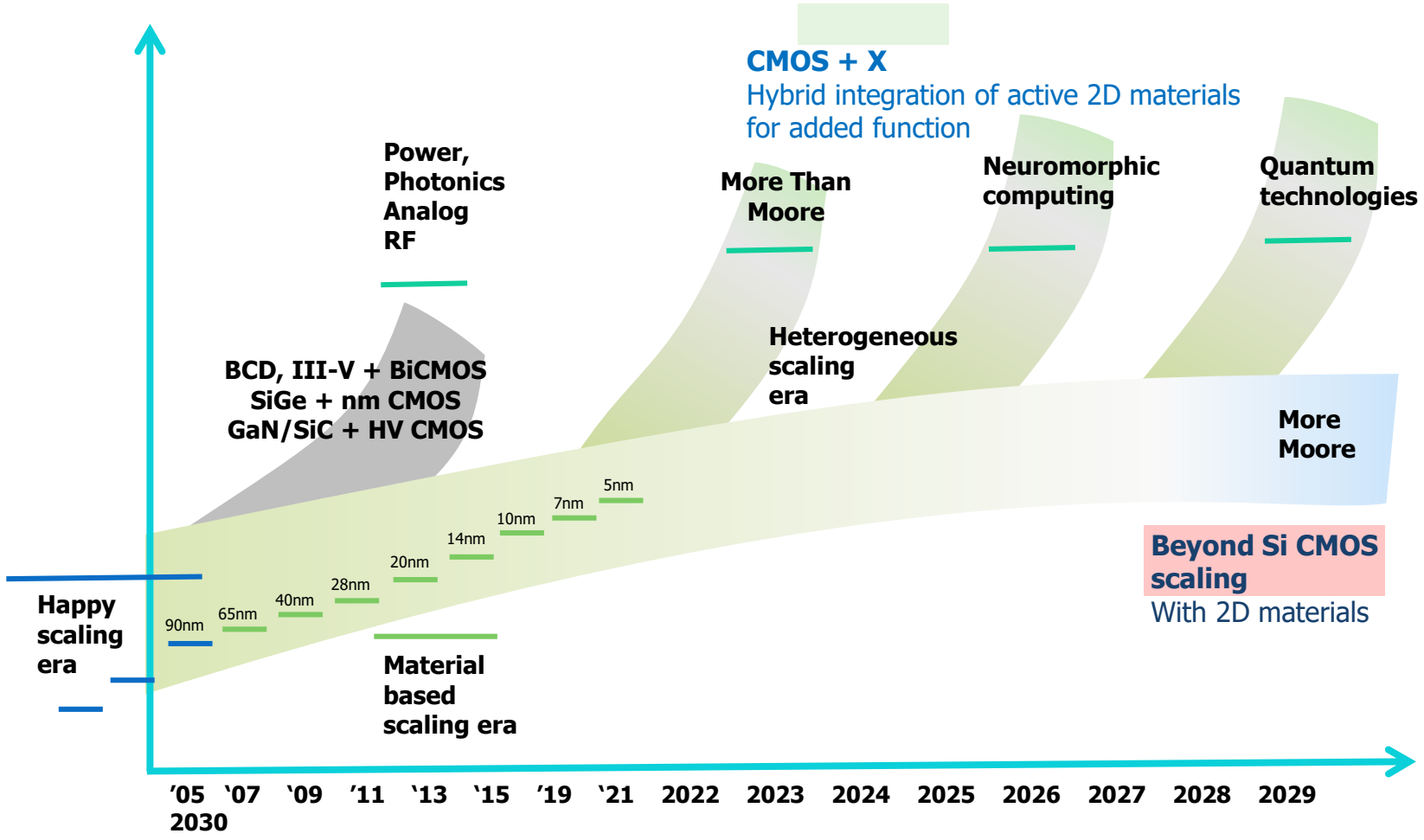


	2020	2030	Top Drivers
Non-memory	$235B	**$678B**	GPUs, MPUs High-end Logic
Memory	$133B	**$467B**	DRAM, HBM, NAND Other Memory
Other ICs	$79B	**$206B**	Discretes, Opto, Analog
Total Semis	$446B	**$1,351B**	NA

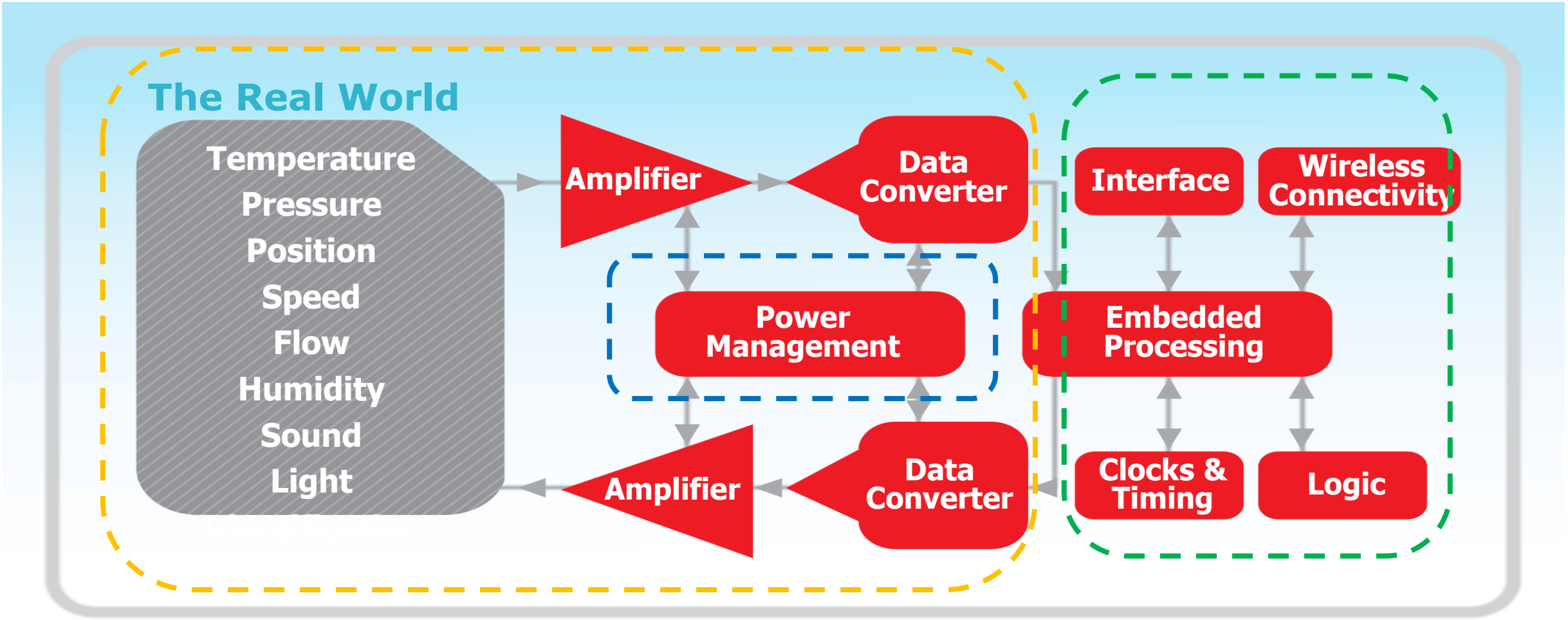
$500B+ in ~70 years → $1T+ in the next ~7 years

CMOS+X: A multipronged innovation

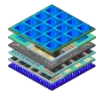
- Scaling and lithography is one of many vector for performance cost optimization
- New materials are critical for enhanced performance



Analog and embedded processing



Individual chips OR SOC or heterogeneous integration of sub-systems



Opportunities to innovate | technology trends

Technology drivers:

Future of Scaling - 3D CMOS+X

Heterogenous Integration/Chiplet

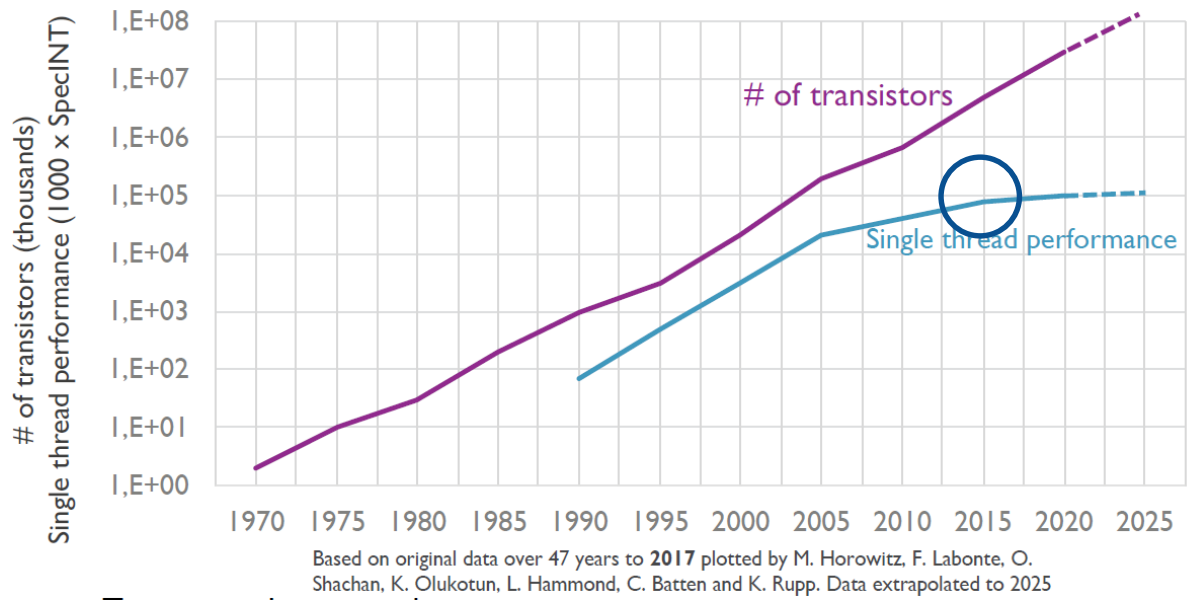
Increasing power density through 3D integration and new materials

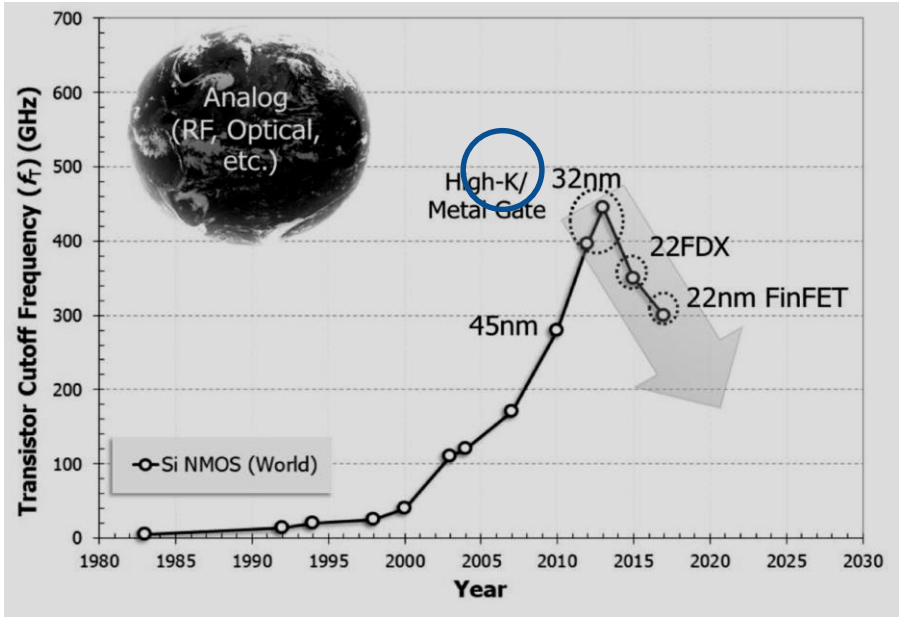
Integration for RF, precision and high speed→ Photonics on Silicon

Sensing and Mechatronics

BEOL processing for differentiation

Why we need to differentiate our vectors of innovation



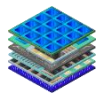


Scaling has already reached it's limits, we need to drive different vectors of innovation: new materials, new devices, hybrid integration.

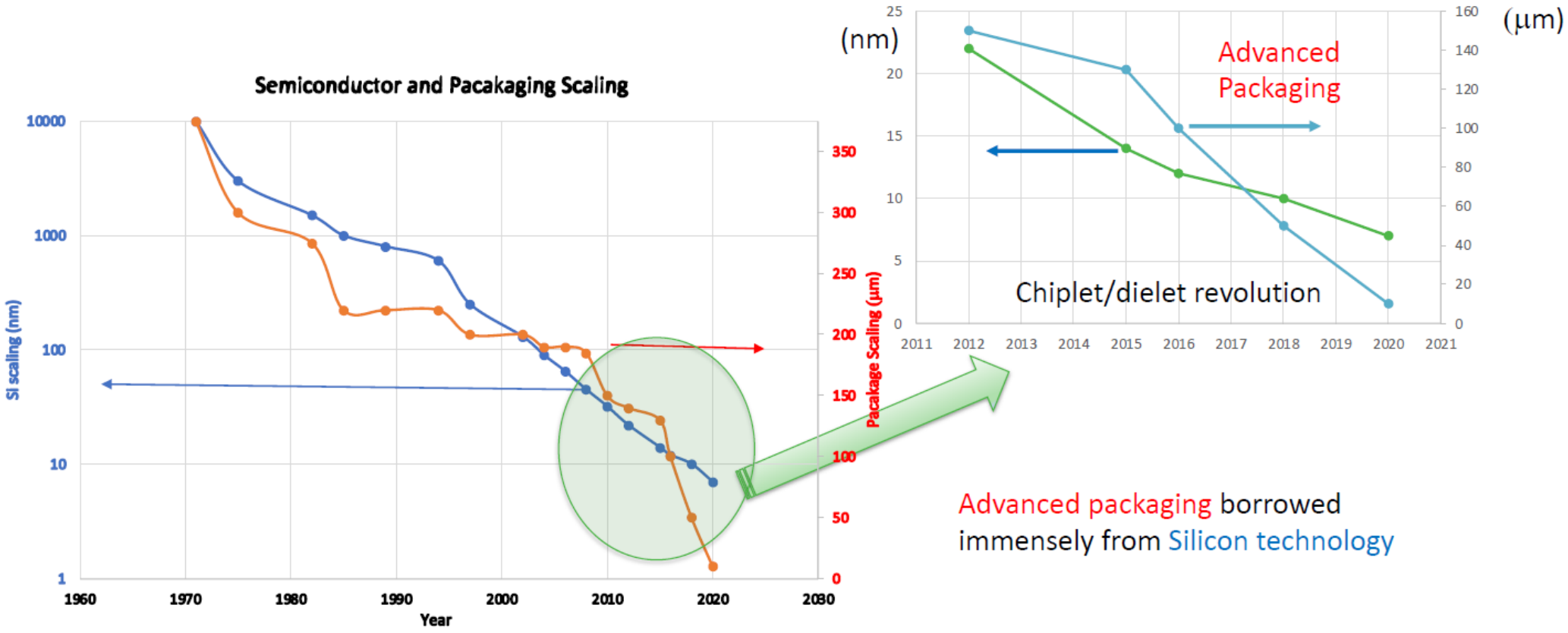
Diverse analog technology portfolio

High-Speed BiCMOS	High-Precision Analog CMOS	High-Voltage Power	High-Density CMOS
• SOI & Bulk • SiGe NPN and PNP • Precision thin film resistors & capacitors • Low parasitic capacitance	• Low power, low parasitic CMOS • Low 1/f noise • Precision thin film resistors and capacitors • Non-volatile memories	• Integrated & discrete power processes for FETs, drivers, converters, controllers and isolation • Broad & multi-voltage capability • Thick metal technology	• Dense, low power CMOS • Analog friendly CMOS • Multi-Vt CMOS • FRAM, Flash, SRAM & other low power, embedded memories

- GaN, GaAs, SiC, ..
- Si FETs
- High voltage isolation
- Sensing
- Photonics
- Embedded memories



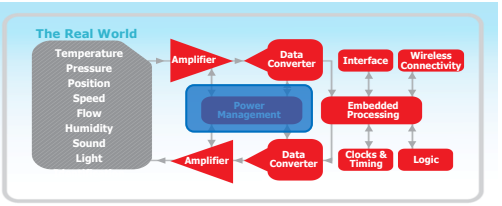
Heterogenous integration | Advance packaging progress



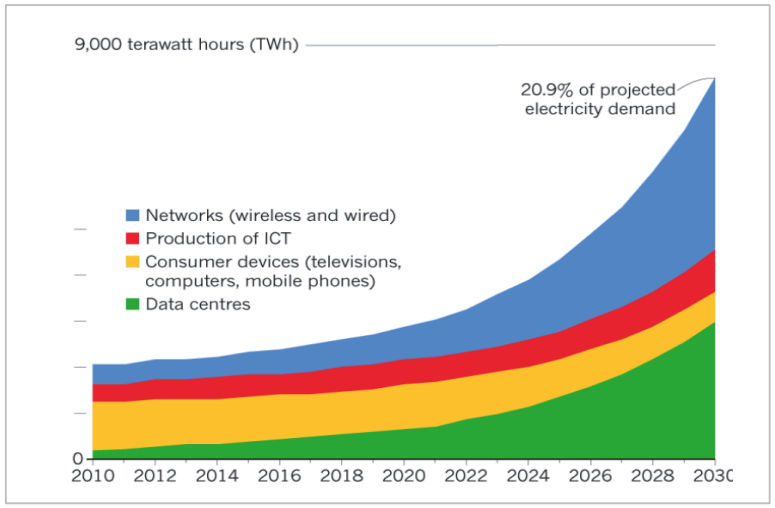
Advanced packaging borrowed immensely from Silicon technology

Courtesy of S.S. Iyer

Driving innovation for value through heterogeneous integration

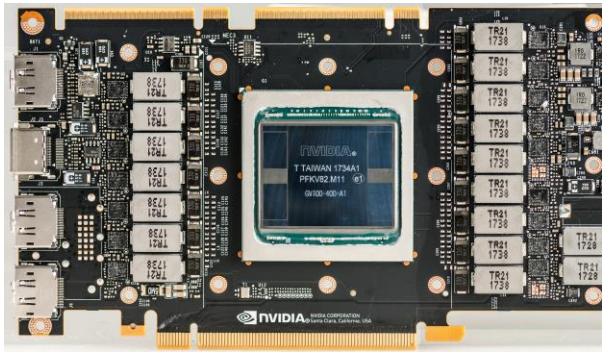


Energy supply and demand



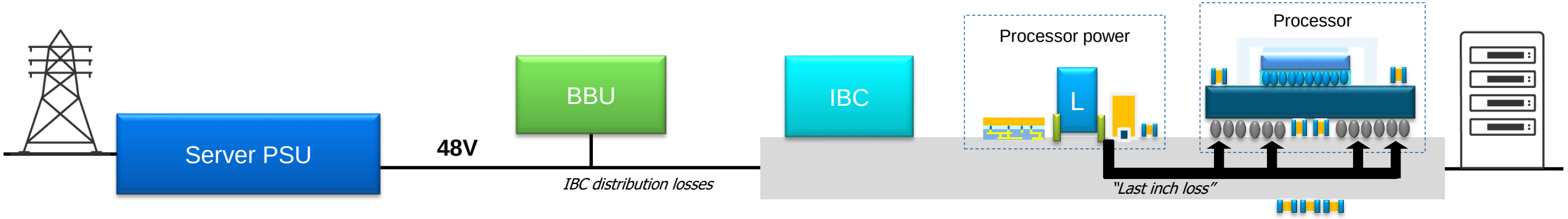
Power per rack

PAST	PRESENT	FUTURE
4-5 kW	10-15 kW	20-40 kW
	80% of current rack power shipped	



Texas Instruments

Powering up next generation of servers



High voltage

Server Power Supply Unit (PSU)

- >20kW future
- Requires thermally-sufficient packages for higher power

Battery Backup Unit (BBU)

- Increasing power levels
- BBU being used for "peak shaving" – efficiency and density matter

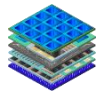
Last inch

Intermediate Bus Converter (IBC)

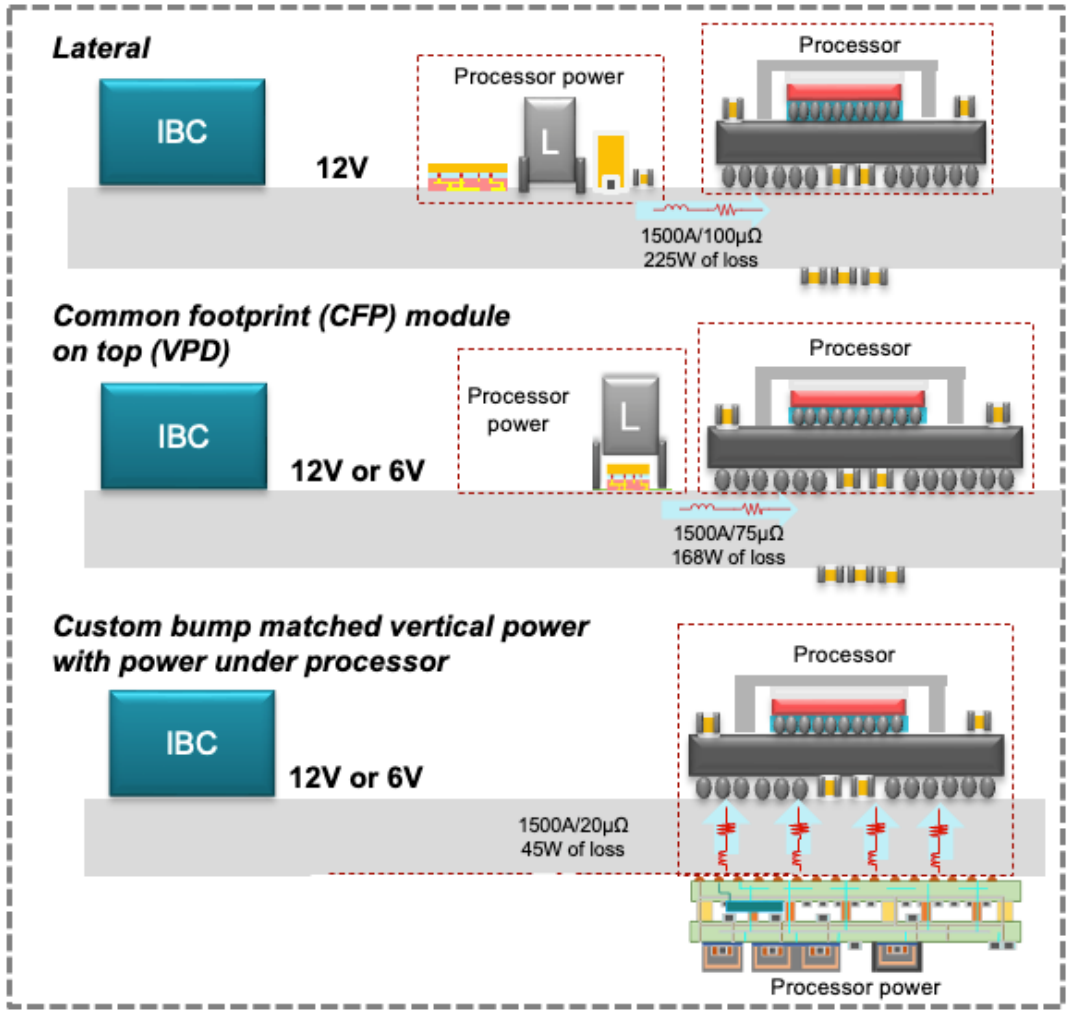
- Higher processor current makes IBC distribution losses high
- 48V modules are adopted

Processor Power

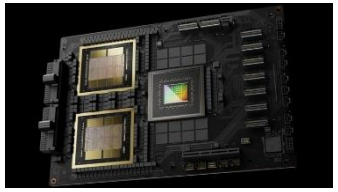
- Processor current is going up rapidly
- New power delivery architectures necessary

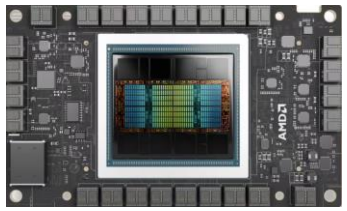


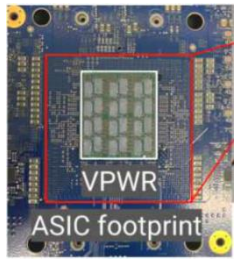
Last inch challenge | power stage evolution



Increasing pwr density







Process
- Higher frequency avalanche free switch
- High density integrated capacitors

Package
- Low inductance package with good thermals
- Custom routability

Materials
- Higher efficiency magnetics
- Lower cost modules
- Enhanced thermals

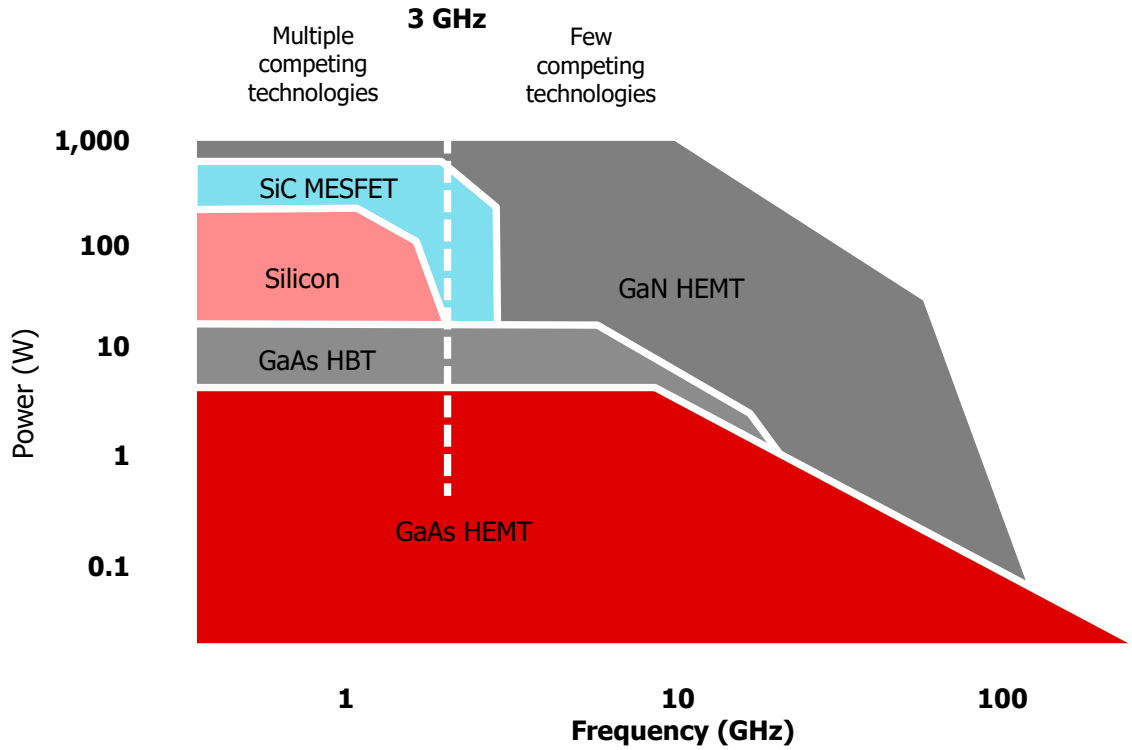
Heterogeneous integration for high-speed applications

Different processes offer unique benefits for high-speed applications. For example

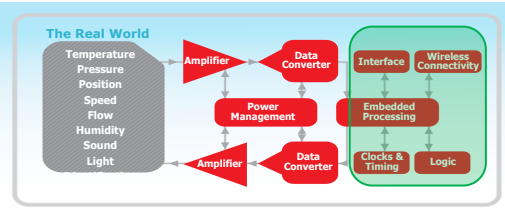
- SiGe → highest speed + swing on silicon
- CMOS → low-power mixed-signal and digital integration
- GaN → wide swings and large output power
- IPDRF → low-loss matching networks and filters
- SiPh → optoelectronic functionality

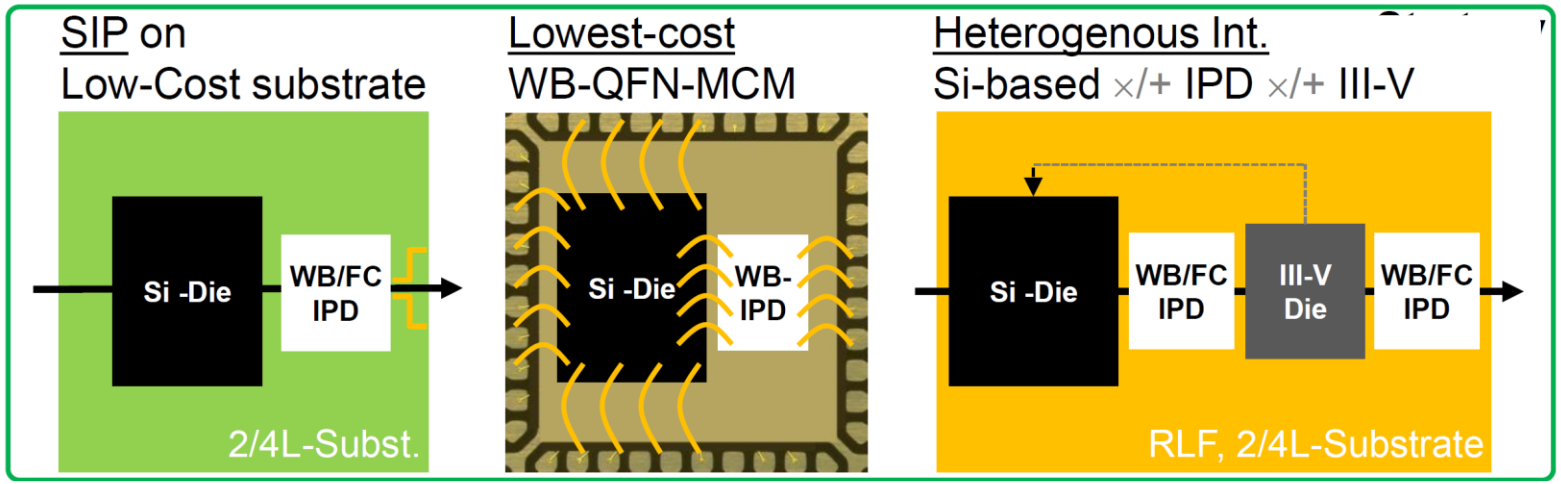
Multi-chip module integration of these combines the features of multiple technologies at highest performance without introducing the losses and bandwidth-limiting parasitics of PCB-level integration.

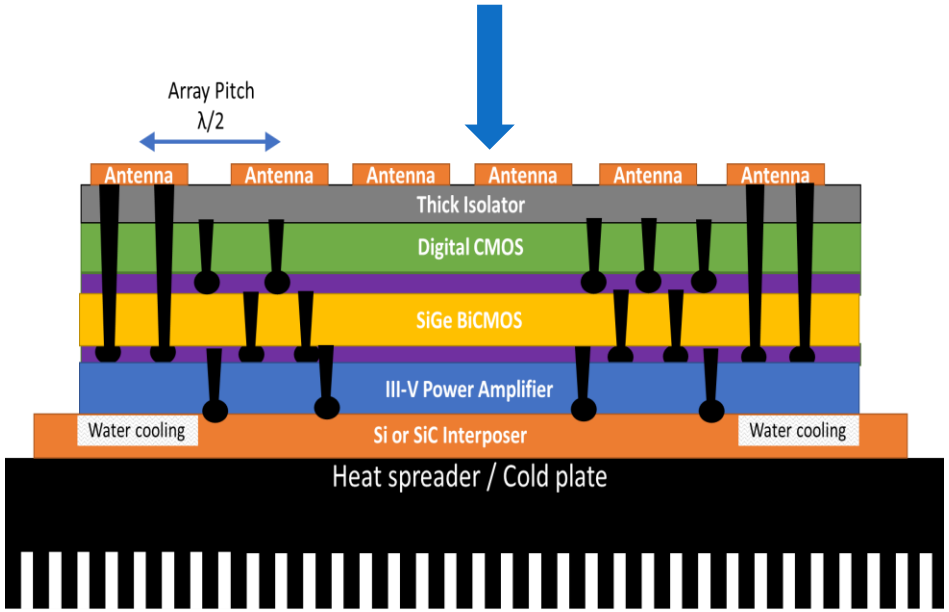
- Can also reduce cost and form factor.



Enhanced radio paths: CMOS/SiGe + IPDRF

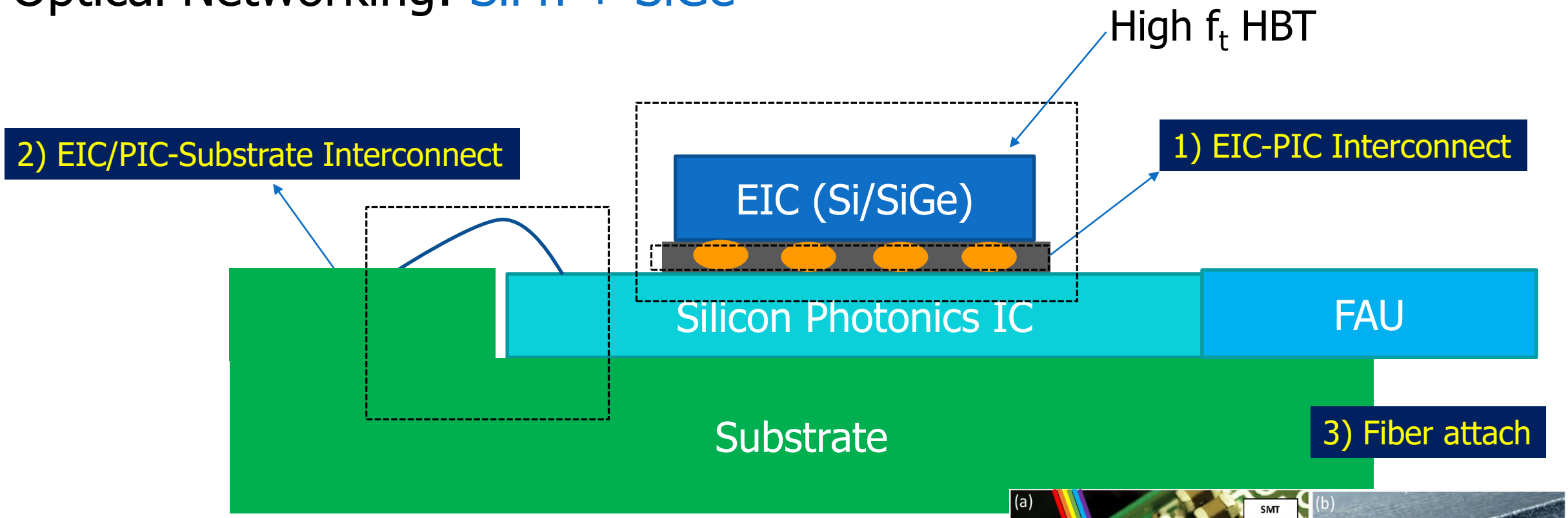




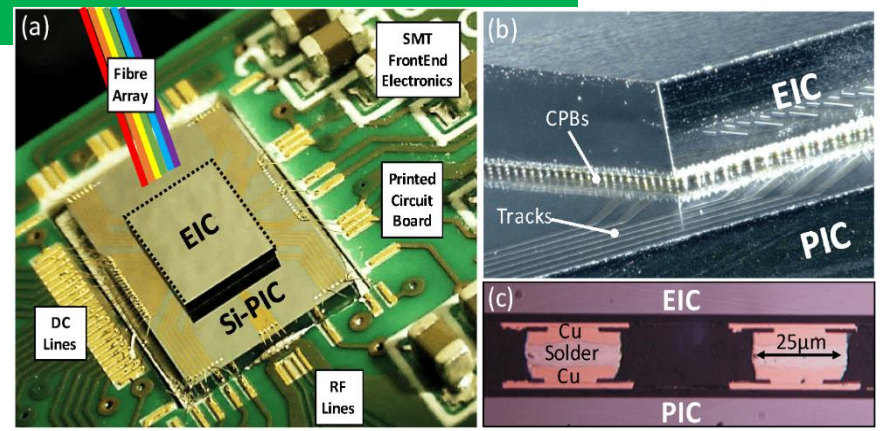


MMIC with RF launcher to waveguide directly from package

Optical Networking: SiPh + SiGe

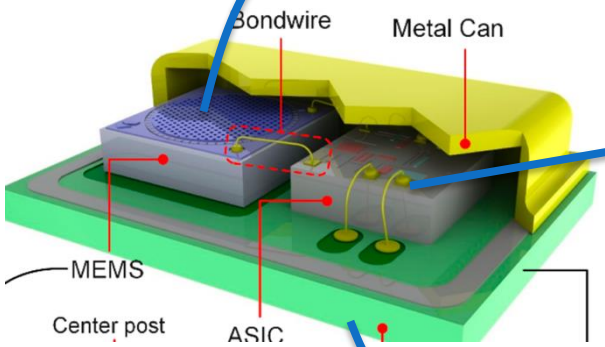


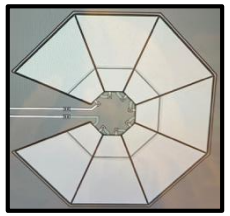
1) EIC-PIC Interconnect w/ <30pH + 25fF
2) EIC/PIC-Substrate Interconnect w/ BW > 110GHz
3) Attach to single mode fiber @ 1310nm



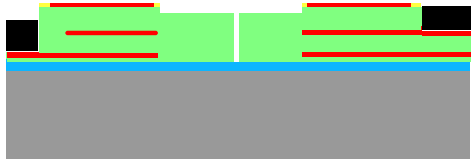
Flip-chip of EIC
on PIC (third party)

MEMS Sensor

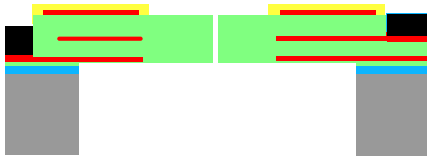




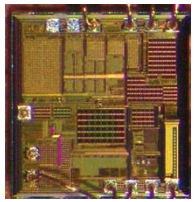
MEMS Die



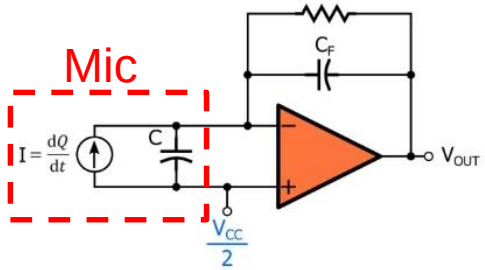
Front-End Process



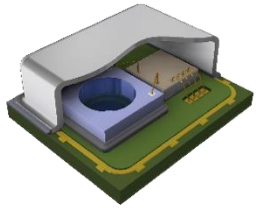
Back-End Process



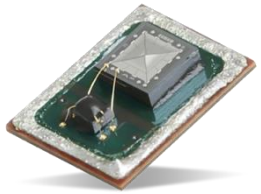
ASIC Die



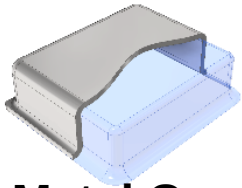
Amp + ADC + Edge AI …



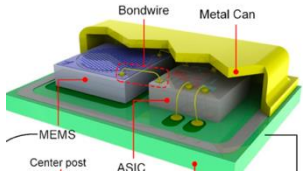
Package



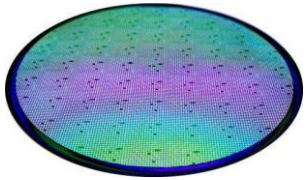
Laminate



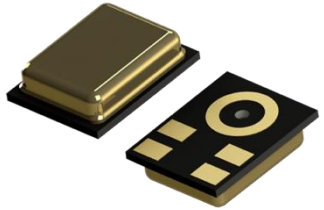
Metal Can



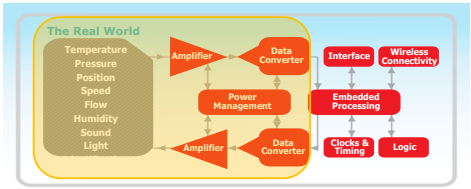
Testing



Wafer-Level



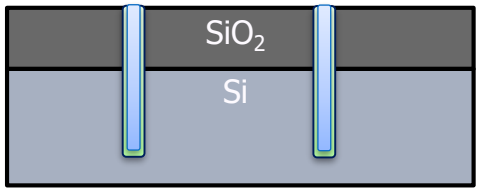
Final Test



Piezo Microphone: Process Flow

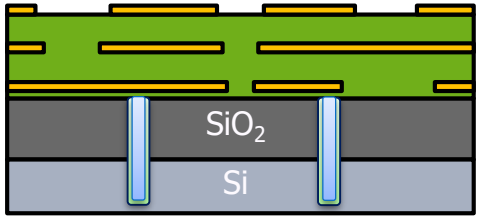
Front-End

1: Deep Trenches



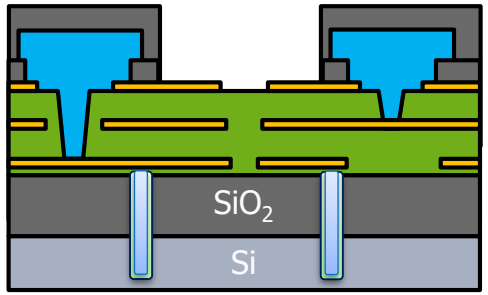
- Deep trenches
- Etch stop and wall def.

2: Piezo Stack Deposition



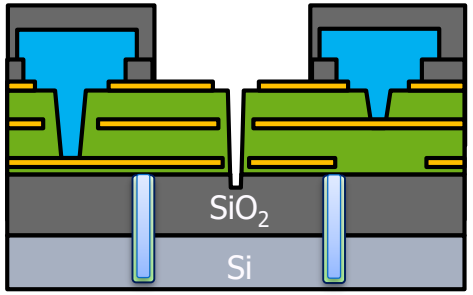
- Bimorph stack dep and pattern
- AlNx based

3: Vias and METF

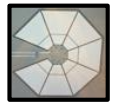


- METF Dep+pattern
- Opening etch

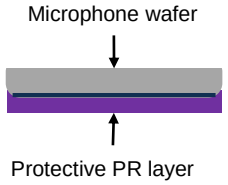
4: Piezo Slit Etch



- Slit Dry etch



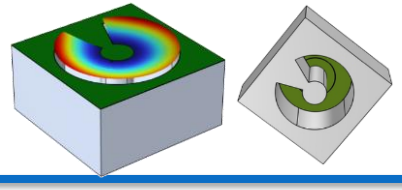
Back-End



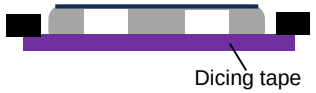
- Backgrind

- Front to Back Pattern

- Si DRIE etching + Ash
- PR layer ash
- HF SiO2 release

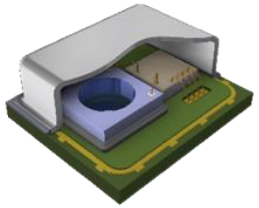


Assembly & Test @ AT Site



- Wafer mount

- Dicing

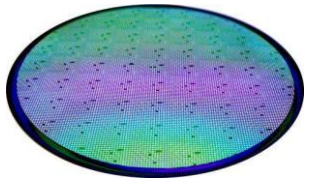


- Assembly

Piezo Microphone: Packaging and Testing

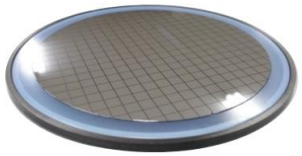
Wafer-Level

Pre-release

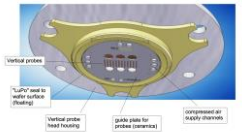


- Fab: Parametric test
- Cap, loss-tangent
- Piezo-coeff (DBLI)

Post-Release*



- Dynamic wafer test
- Specialty probers

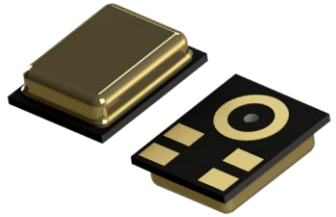


Vertical probe head for MEMS pressure sensor probing

24-DUT low force vertical probe card for MEMS microphone

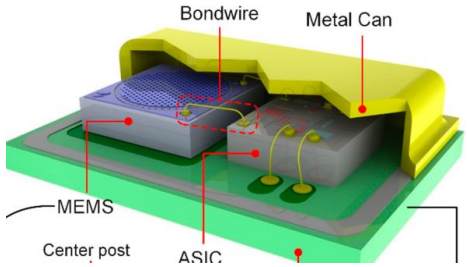
*Can be skipped (FT Yield).

Final Test

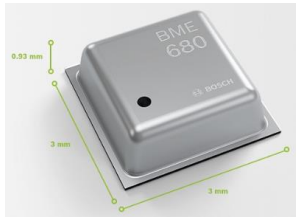


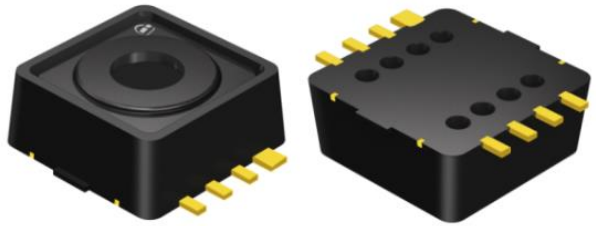
- Electrical self-test
- Test handler
- MEMS Dynamic test

Metal Can Package



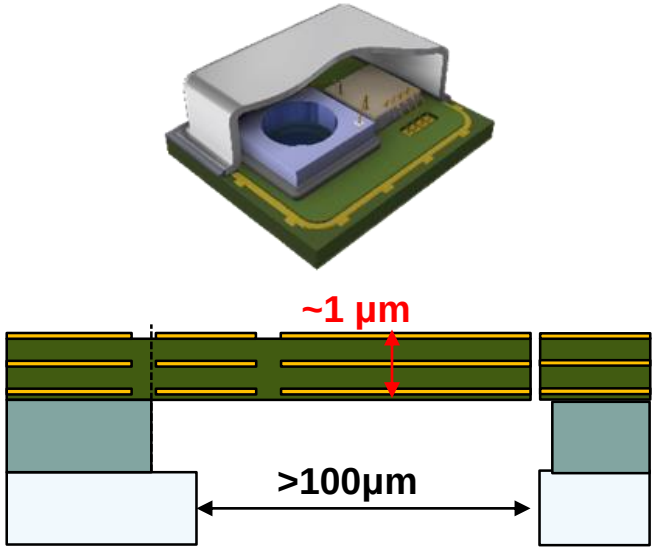
- Air tight package
- EMI shielding
- Die to package wirebond





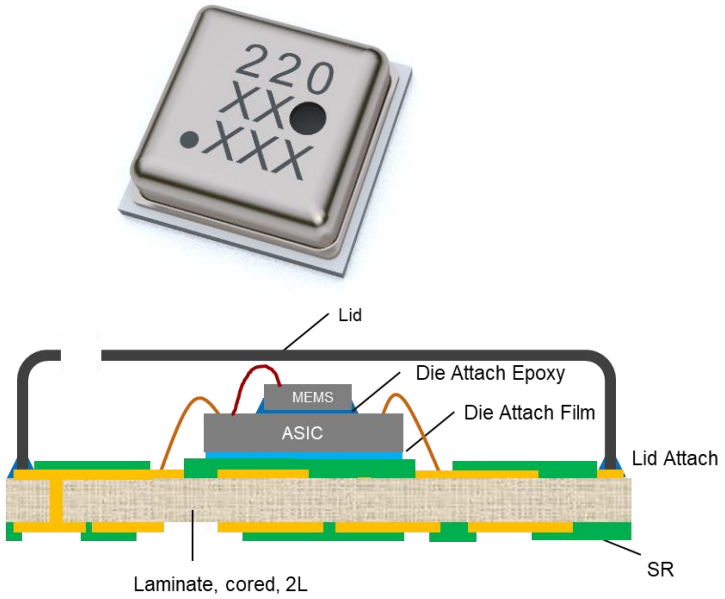
Metal Lid Package: MEMS Applications

Piezo Microphone



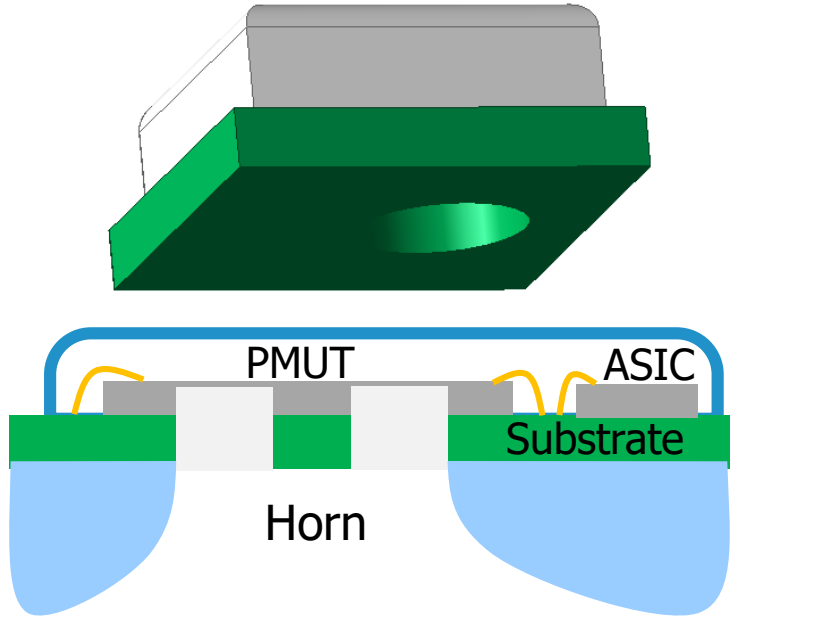
- Piezo membrane

Pressure Sensor



- Capacitive transducer

Ultrasound ranging



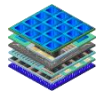
Heterogenous back-end-of-line integration

Post fab processing

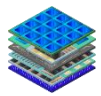
- MEMS Structures
- Passive Integration
- Active Integration

- Photonic Sensor Array
- Biosensors

- Active 2D & 1D materials
- Direct Heteroepitaxy
- III-V on CMOS BEOL
- Metal Oxide Active Devices



- Technology diversification is accelerating semiconductor innovation
- Heterogeneous integration is urgent and more critical than ever for system optimization
- Advanced packaging leveraging front end techniques imperative to push performance at viable cost



THANK YOU