HR0011SB20254-05
ON-CHIP WAVELENGTH GENERATION FOR DWDM PHOTONIC TRANSCEIVERS
Frequently Asked Questions (FAQs)

1. Which Phase II metrics (λ count, per-channel rate, energy / bit, link margin, etc.) are considered *threshold* versus *objective*?
   A: There is no distinction between *threshold* versus *objective* metrics.

2. May we trade channel count against per-channel data rate if aggregate bandwidth is met?
   A: The main goal of the program is on-chip wavelength generation. Approaches that do not demonstrate high wavelength count are of limited interest.

3. How much additional link margin should we budget for temperature, vibration, and aging effects?
   A: Additional link margin above 2 dB is not specified. When making determination, the small business should consider product viability within the targeted application space.

4. What minimum OSNR, RIN, or other signal-quality specifications do you require per channel?
   A: Not specified. The noise requirements should be derived from a link model for a link achieving the targeted BER.

5. Do you prefer microcomb generators, integrated laser arrays, or are both acceptable if performance metrics are achieved?
   A: Both approaches are considered equally acceptable.

6. What comb linewidth, channel-power flatness, and long-term wavelength stability do you expect?
   A: Not specified. The comb characteristics should be derived from a link model for a link achieving the targeted BER <u>on all channels</u>. Any required stabilization and/or equalization of the lines should be addressed in the system architecture.

7. What are the acceptable pump-laser parameters (wavelength, output power, linewidth, package) and maximum allowed fiber-coupling loss?
   A: Not specified. Provided that a pump laser is needed, any pump laser that enables the proposed solution is acceptable. The only requirement is that the pump laser is commercially available off-the-shelf component.

8. Can you confirm that only COTS pump lasers are permitted, with no exceptions?
   A: Yes. This SBIR program targets innovation in on-chip wavelength generation. Any external (off-chip) components should be widely available and preferably – low cost. The proposers can use their own pump laser as long as it is made commercially available as a COTS product and is unlikely to become a supply chain limiter.

9. Are III-V-on-Si or heterogeneous wafer-bonding flows acceptable, and must they be run in a trusted U.S. foundry?
   A: Yes, these are acceptable approaches. The use of a domestic foundry is preferable but not required. A trusted foundry certification is not required.

10. Is the ≤ 0.5 dB die-to-die optical loss limit absolute, or could active alignment allow some relaxation?
    A: This is intended to account for surface coupling from heterogeneously bonded integrated laser arrays and should be readily achievable. Multiple PICs and PIC-to-PIC edge coupling is not envisioned and should not be pursued.

11. Are there limits on PIC die size, reticle stitching, or TSV density that could constrain photonic routing?
    A: No, there are no limitations.

12. Which modulation format (NRZ, PAM-4, coherent) and FEC assumptions should we target?
    A: The modulation format is not specified but it will likely be determined by the energy per bit metric. Light FEC is not excluded as long as it is fully accounted for in the energy per bit estimation.

13. Does DSP-based equalization count toward the 3 pJ/bit energy budget?
    A: Yes. Heavy-handed DSP approaches are generally discouraged.

14. What PRBS length and measurement method will you use to verify the 10^{-12} BER requirement?
    A: This is not specified. Any reasonable measurement approach will be considered.

15. Which UCIe revision, lane count, and maximum SerDes power per Gbps should we design to?
    A: Not specified. The proposers should be guided by market demand.

16. Will a simulated UCIe interface suffice, or do you need hardware proof-of-concept in Phase II?
    A: Simulated UCIe interface is sufficient.

17. What mechanical I/O constraints (interposer pitch, fiber-connector standard, heat-sink footprint, module height) should we observe?
    A: Not specified. The proposers should be guided by market considerations.

18. Are organic substrates or co-packaged-optics modules acceptable alternatives to 2.5-D interposers?
    A: There are no requirements or constraints for the packaging solution.

19. What operating temperature range, thermal cycling, shock/vibration, and radiation-hardness levels must the prototypes withstand?

A: Not specified. The end goal is a minimum viable product that satisfies the targeted market identified by the performer.

20. What lifetime (MTTF) target and qualification standards should we plan for?
    A: Not specified. The end goal is a minimum viable product that satisfies the targeted market identified by the performer.

21. Will DARPA supply calibrated pump lasers, reference receivers, or test fixtures for validation, or must we provide all test equipment?
    A: All test equipment is provided by the performer.

22. What acceptance-test conditions (fiber length, channel mask, eye-mask specs) will apply to the packaged prototypes?
    A: An in-house demonstration of a functioning link with the required link margin and stable BER is sufficient for acceptance.

23. Is there flexibility on the PIC/EIC tape-out by Month 6 and the integrated demo by Month 18 milestones?
    A: Small deviations from the schedule for intermediate milestones are generally acceptable. However, *Phase II Option* for packaged prototypes will not be considered and/or awarded until a successful demonstration of the integrated demo of the multi-wavelength transceiver.

24. Would a single multi-project-wafer tape-out meet your expectations?
    A: Yes.

25. May we combine SRR, PDR, and CDR reviews to streamline the schedule?
    A: A System Requirements Review (SRR) is mandatory at Phase II kickoff. Other reviews can be combined, however DARPA expects technical reviews (QPRs) to be held on a regular quarterly basis. Payment for milestones is subject to acceptance by the Government of the required deliverables and reports.

26. Is contingency funding available for high-risk process splits or backup tape-outs?
    A: Additional funding is not available.

27. What timeline and performance roadmap do you expect for scaling to ≥ 4 Tb/s per die in follow-on efforts?
    A: DARPA anticipates that the proposed architectures are scalable to 4T and beyond by replication of the number of fiber ports. Specific follow-on effort is not identified at this time.

28. Are you interested in future wavelength bands (e.g., L-band) or tighter grid spacings (< 100 GHz)?
    A: No.

29. How will the prototypes be classified under ITAR/EAR, and are there trusted-fabrication requirements?
    A: It is the performer's responsibility to be compliant with any ITAR/EAR regulations. There is no requirement for trusted manufacturing.

30. Which data-rights assertions (e.g., SBIR unlimited vs. restricted) do you prefer for design files and process parameters?
    A: There is no preference or requirement.

31. Which DoD programs or platform classes are the primary transition targets for these prototypes?
    A: Specific DoD transition path is not identified at this moment. The developed technology is intended as dual use.

32. Do you have minimum production cost or annual volume targets that should guide our design-for-manufacture strategy?
    A: No. There are no specific targets. There is an expectation that the performer would develop own targets based on the Market Study Report due in Phase II.

33. What form and level of detail should the market study and commercialization plan include?
    A: There is no specific format. The performers are encouraged to seek guidance through the Transition & Commercialization Support Program (TCSP) at https://www.darpa.mil/work-with-us/communities/small-business/transition-commercialization.