Super-resolution Thermal Metrology for High Power Density Devices

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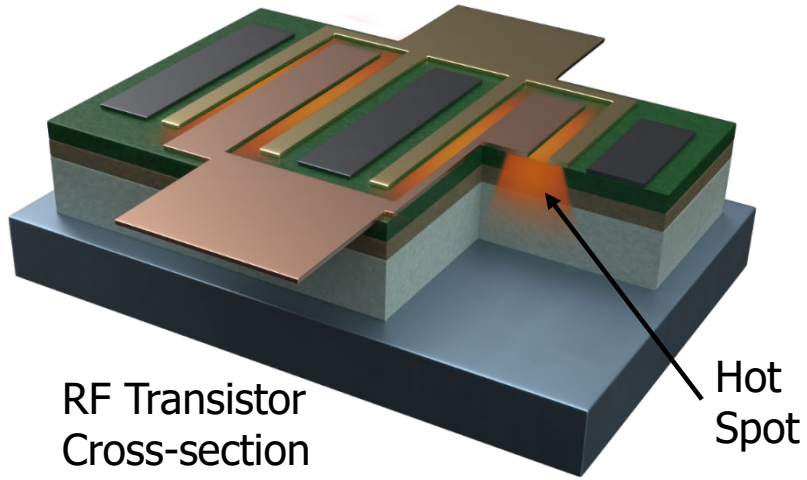
Proposers Day

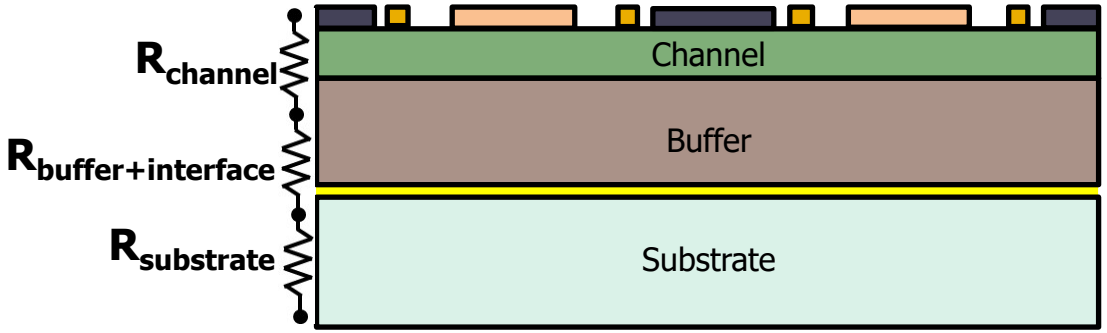
Super-resolution Thermal Metrology for High Power Density Devices

Background:

- Performance improvements to radar and communication systems require increasing the output power density of transistors used in transmitter power amplifiers
- Output power densities of today's wide bandgap transistors are thermally limited to values substantially below theoretical electronic limits
- The government seeks to overcome transistor thermal limitations and realize robust, high-power density devices by:
  - Reducing transistor thermal resistance to achieve high power density
  - Using thermal metrology to accurately measure thermal resistance and interfacial thermal resistance



Transistor Thermal Resistance



Objective: Develop a super-resolution thermal metrology tool to characterize the thermal resistance of semiconductor materials, heterostructures, and devices at nanometer length scale

Innovation of Super-resolution Thermal Metrology Tool

- Measuring thermal resistance beyond the surface film (i.e., in the buried channel layer of a heterojunction device) and characterizing at both nanoscale and microscale dimensions is critical to the development of high power density devices
  - Existing pump-probe laser-based techniques are limited in spatial resolution and cannot measure thermal resistance and thermal resistance gradients in sub-micron devices
- Goal of this Small Business Innovation Research (SBIR)
  - Develop super-resolution thermal metrology tool to accurately measure thermal resistance of materials, heterostructures, and devices, with emphasis on wide bandgap/ultra-wide bandgap material systems
  - Develop and implement comprehensive validation plan
  - Deliver automated, turnkey thermal metrology tool to a designated U.S. government organization
- <u>Requirements of super-resolution thermal metrology tool</u>:
  1. Capable of measuring thermal resistance, thermal boundary resistance, and temperature of operating multi-finger, submicron GaN HEMT and ultra-wide bandgap AlGaN HEMT with the following specifications:
     1. Spatial resolution < 50 nm
     2. Thermal resolution < 0.25 ^{o}C
     3. Thermal precision: 1 ^{o}C
     4. Accuracy > 90%
     5. Reproducibility and repeatability < 2%
  2. Tool validation using a comparison of measured results of device relevant structures to other thermal metrology techniques. In addition, validation may use available NIST standards.

Schedule and Milestones

Phase 1

This SBIR will be a "Direct to Phase 2" effort

- Proposers should demonstrate Phase 1 feasibility by providing documentation of existing thermal metrology capabilities, including measured data, such as thermal resistance, that demonstrates less than 2 μm spatial resolution and the ability to resolve interfaces beyond the surface film. In addition, validation data from the existing thermal metrology tool should be provided.

Phase 2 (base)

Phase 2 consists of an 18-month period with the following goals:

- Super-resolution thermal metrology tool will be designed, developed, validated, and tested for performance goals

Phase 2 (base) milestones

- Month 1: Detailed report on super-resolution thermal metrology tool design, including documentation of path towards achieving in-situ device testing and meeting DP2 SBIR goals.
- Month 3: Report on progress towards final design and demonstration of thermal metrology tool.
- Month 6: Report on progress towards final design and demonstration of thermal metrology tool.
- Month 9: Report on progress towards final design and demonstration of thermal metrology tool.
- Month 12: Initial prototype demonstration of super-resolution thermal metrology tool. Detailed report should include validation data as well as thermal resistance, temperature, and thermal resolution of the surface and cross-section of GaN and AlGaN transistors with less than 100 nm spatial resolution. Documentation should also describe the path towards the final DF2 SBIR deliverable.
- Month 15: Detailed report on progress towards final design and demonstration of the thermal metrology tool, including validation data and transistor thermal characterization.
- Month 18: Final demonstration of a prototype thermal metrology tool that meets requirements listed above. Detailed data report containing final validation measurements and thermal characterization of surface and cross-section of GaN and AlGaN transistors with less than 50 nm spatial resolution. Plan for construction of tool and delivery to a U.S. government organization.

Schedule and Milestones

Phase 2 (option)

The Phase 2 will have a 6-month option with the following goals:

- Successful demonstration of a fully-automated measurement of the thermal resistance, thermal boundary resistance, temperature, and thermal resolution of an operating multi-finger, submicron GaN HEMT and ultra-wide bandgap AlGaN HEMT.
- Tool Delivery:
  - Delivery of prototype automated, turnkey thermal metrology tool to a designated U.S. government organization.
  - Support for installation and operation at the U.S. government laboratory.
  - Demonstration of thermal characterization of GaN HEMT and ultra-wide bandgap AlGaN HEMT on-site at the U.S. government organization.

Phase 2 (option) milestones

- Month 1: Detailed report on automated, push-button thermal metrology tool design and path toward achieving DP2 Option goals. Coordinate with the designated U.S. government organization to provide a preliminary plan for delivery and installation.
- Month 3: Report on thermal metrology tool development progress.
- Month 6: Delivery of final prototype thermal metrology tool, including calibration standards and any necessary software for demonstrating material and device thermal characterization. Detailed report containing final validation measurements and thermal characterization of surface and cross-section of GaN and AlGaN transistors with less than 50 nm spatial resolution.

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