Small Business Innovation Research (SBIR) and
Small Business Technology Transfer (STTR)
Opportunity Announcement
HR001120S0019-11
N-polar GaN mm-wave Power Electronics on Sapphire

Which program will fund this topic?
SBIR

What type of proposals will be accepted?
Direct to Phase II (DP2) Only

Technology Area(s): Materials/Processes
DARPA Program: DREaM

I. INTRODUCTION

The Defense Advanced Research Projects Agency (DARPA) Small Business Programs Office (SBPO) is issuing an SBIR/STTR Opportunity (SBO) inviting submissions of innovative research concepts in the technical domain(s) of Materials/Processes. In particular, DARPA is interested in understanding the feasibility of N-polar GaN mm-wave Power Electronics on Sapphire.

This SBO is issued under the Broad Agency Announcement (BAA) for SBIR/STTR, HR001120S0019. All proposals in response to the technical area(s) described herein will be submitted in accordance with the instructions provided under HR001120S0019, found here: https://beta.sam.gov/opp/b8abeb02f16a4450b2c2f859fc00c177/view.

a. Eligibility

The eligibility requirements for the SBIR/STTR programs are unique and do not correspond to those of other small business programs. Please refer to Section 3.1, Eligible Applicants, of HR001120S0019 for full eligibility requirements.

b. Anticipated Structure/Award Information

Please refer to Section 1, Funding Opportunity Description provided in HR001120S0019 for detailed information regarding SBIR/STTR phase structure and flexibility.

If a proposer can provide adequate documentation to substantiate that the scientific and technical merit and feasibility described in the Phase I section of the topic has been met and describes the potential commercial applications, the Direct to Phase II (DP2) authority allows the Department of Defense (DoD) to make an award to a small business concern under Phase II of the SBIR program without regard to whether the small business concern was provided an award under Phase I of an SBIR program. This SBO is accepting DP2 proposal submissions.

DARPA will accept DP2 proposals for cost of up to $1,750,000. This includes an 18-month base period not to exceed a cost of $1,000,000 and a 12-month option period not to exceed a cost of $500,000. A separately priced option of up to $250,000 must also be proposed for contractors who would like to be considered for participation in the DARPA Entrepreneurial Investigator Initiative. Refer to Section 2.6, DARPA Embedded Entrepreneur Initiative, of HR001120S0019 for detailed information on EEI.

Proposers should refer to Section 4, Application and Submission Information, of HR001120S0019 for detailed proposal preparation instructions. Proposals that do not comply with the requirements detailed in HR001120S0019 and the research objectives of this SBO are considered non-conforming and therefore are not evaluated nor considered for award.

DP2 Feasibility Documentation shall not exceed 20 pages. DP2 Technical Proposal shall not exceed 40 pages. Phase II commercialization strategy shall not exceed 5 pages. It should be the last section of the Technical Volume and will not count against the 40-page limit. Please refer to Appendix B of HR001120S0019 for detailed instructions on DP2 proposal preparation.

c. Evaluation of Proposals

Section 5, Evaluation of Proposals, in HR001120S0019 provides detailed information on proposal evaluation and the selection process for this SBO.

d. Due Date/Time

Full proposal packages (Proposal Cover Sheet, Technical Volume, Price/Cost Volume inclusive of supporting documentation, and Company Commercialization Report) must be submitted via the DoD SBIR/STTR Proposal Submission website per the instructions outlined in HR001120S0019 no later than **2:00 pm ET, August 10, 2020.**

II. TOPIC OVERVIEW

a. Objective

This topic seeks to establish manufacturable N-polar GaN on sapphire epitaxy technology for high power, high efficiency radio frequency (RF) power amplifier applications at W-band. The developed epitaxial materials will be used to demonstrate transistors with ≥ 5 W/mm CW output power density at 94 GHz on a large diameter (≥ 150 mm) wafer with a thermal solution that will pave the way for future development of kW-class semiconductor power amplifiers operating in the mmW and THz regime. The developed technology is expected to enable the next generation of wide band gap high power mm-wave and THz electronics.

b. Description

Over the past decade, defense investments in the advancement of Gallium Nitride (GaN) technology have helped enable the delivery of high power RF signals at higher frequencies, bandwidths, and efficiencies. Today, a vast number of GaN RF amplifiers are used in many commercial and military systems from everyday smartphones to radar sensors in lower microwave frequencies. The growing applications are driving wireless

operating frequencies into the mm-wave and THz regime which requires high transmit power in small form factors. However, current high power semiconductor devices have low power density, poor efficiency, and inefficient thermal management when operating at in the mm-wave and THz regime. This causes severe degradation of output power and energy efficiency of the mm-wave amplifiers, as it is very challenging to combine low power devices together with lossy combiners in tightly spaced radiating elements to form monolithic microwave integrated circuits (MMICs) and arrays. As a result, new epitaxial materials and device structures are required to provide high power density and efficiency at mm-wave frequencies such as at W-band (94 GHz).

Promising transistor performance in the mm-wave range has been shown by devices fabricated on GaN epitaxial materials grown on SiC substrates. The SiC substrates are expensive and challenging to scale to large wafer size to attain high array-scale integration level at manufacturing scale with low cost. Recent laboratory N-polar GaN on sapphire devices delivered promising high breakdown voltage for high density power electronics with low RF dispersion as well as demonstrated good power density at W-band. The combination of low defect density GaN epitaxial material on low cost large size sapphire substrates would be a potential technology to manufacture mm-wave amplifiers and arrays for high volume commercial and defense applications. However, the experimental GaN on sapphire mm-wave devices were not engineered for good thermal performance, preventing large scale integration to implement high power mm-wave MMICs.

DARPA is seeking innovative epitaxial layer structures, heteroepitaxial growth, and fabrication processes that would provide N-polar GaN on sapphire transistors with both high breakdown voltage and good RF performance at W-band (94 GHz). The approach should focus on scaling existing N-polar GaN on sapphire approaches to large wafer diameters, of 150 mm or greater, developing low resistance contacts, scaling the gate length, and demonstrating fabrication processes required for future wafer-scale MMIC and array implementation, such as via hole creation. The approach should include thermal management techniques that maintain the device junction temperature below 200°C when operating at high output power in densely integrated MMIC and array environment operating at 94 GHz. The demonstrated device should have an output power density of ≥ 5 W/mm, PAE of ≥ 25%, operate at 94 GHz and must be fabricated on N-polar GaN on sapphire wafers with a diameter of 150 mm or greater. While this topic focuses on demonstrating performance at the transistor level only, the manufacturing process and device technology on large low cost sapphire substrate developed in this program will enable future efforts for production of wafer-scale mm-wave MMICs and arrays.

c. Phase I

Previous Phase I qualified efforts should have demonstrated an initial epitaxial growth, device design with analysis and simulations to produce GaN on Sapphire transistors with power densities of over 5 W/mm at 94 GHz with low dispersion. Early growth characterization should exhibit material quality and defect density heteroepitaxy of N-polar GaN on sapphire substrate sufficient to project the material quality for the scaled-up

large wafer dimensions at ≥ 150 mm. Initial N-polar GaN on Sapphire transistors should demonstrate the mm-wave power performance metrics at W-Band specified below:

Demonstrated Phase I Metrics:
• GaN on Sapphire Transistor Minimum CW Output Power Density: 3 W/mm
• Operating Frequency: 94 GHz
• Peak PAE: ≥ 20%

Proposers interested in submitting a Direct to Phase II (DP2) proposal must provide documentation to substantiate that the scientific and technical merit and feasibility described above has been met and describes the potential commercial applications. Documentation should include all relevant information including, but not limited to: technical reports, test data, prototype designs/models, and performance goals/results. For detailed information on DP2 requirements and eligibility, please refer to Section 4.2, Direct to Phase II (DP2) Requirements, and Appendix B of HR001120S0019.

d. Phase II

The Phase II effort consists of a Phase II Base of 18 months and a Phase II Option of 12 months.

Phase II Base (18 months)
The performer shall develop an efficient, high power W-band N-polar GaN transistor structure on ≥ 150 mm sapphire substrates. The base effort should focus on design and development of the epitaxial stack and initial comparison of thermal resistance of the stack as compared to a traditional GaN on SiC structure. The base effort should include materials growth, device design, fabrication, and RF characterization of the N-polar GaN transistors on ≥ 150 mm sapphire wafers. The base deliverables should include on-wafer test data meeting the metrics specific below and fabricated transistor dies for evaluation by the U.S. Government. The successful demonstration of the performance metrics of the base effort will enable a follow-up optional task to implement the process with higher yield, optimize the fabrication to create a fully packaged device, and develop complimentary processes required for future MMIC implementation.

Key Metrics:
• Minimum wafer diameter: 150 mm GaN on Sapphire substrate
• Operating Frequency: 94 GHz
• Minimum CW Output Power Density: 5 W/mm
• Peak PAE: ≥ 25%
• RC: < 0.1 Ω·mm

i. Schedule and Milestones/Deliverables:

- Month 2: Initial report on epitaxial stack, materials growth, and contact metallization to build the first generation N-polar GaN on sapphire transistor.
- Month 6: Interim report describing fabrication processes developed and the results of short-loop growth, fabrication, and measurement of N-polar GaN epitaxial

device layers on ≥150 mm sapphire substrates to evaluate contact resistance, thermal resistance, and defect density.

- Month 12: Report on first device iteration, providing DC characteristics and contact resistance data with initial mm-wave power efficiency, output power, power density of fabricated transistors at 94 GHz.
- Month 17: Demonstration of the prototype GaN on sapphire transistor, evaluation against all Phase II metrics, and delivery of twelve transistor dies to the US Government for validation.
- Month 18: Final Phase II Report summarizing results of the demonstration and including the final architecture, comparison with alternative state-of-the-art methodology, load-pull characterization, and any other relevant materials parameters measured, such as defect density and transistor dispersion.

Phase II Option (12 months)
The performer shall develop the high power mm-wave GaN on Sapphire technology for manufacturability and packaging by introducing through-substrate-vias, resulting in a process with high uniformity in active devices and passive vias on a large substrate.

Key Metrics:
• Wafer minimum diameter: 150 mm GaN on sapphire
• Operating Frequency: 94 GHz
• Minimum CW Output Power Density: 5 W/mm
• Peak PAE: ≥ 25%
• Device temperature: Junction temperature of 200 °C at Pout of 5 W/mm
• Passive components: Through-substrate vias
• Uniformity: > 50% yield to meet the power and efficiency metrics from 25 sampled transistors on the wafer; > 80% yield of through-substrate vias

ii. Schedule and Milestones/Deliverables:
Implement high power, efficient mm-wave devices on a scalable substrate

- Month 19: Initial report on scaling to larger substrate size ≥ 150 mm, planned device optimization, and fabrication processes required for future MMIC development, such as a manufacturable via process in ≥ 150 mm diameter sapphire wafers.
- Month 25: Report describing transistor iteration on ≥ 150 mm wafer size, including device yield and RF characterization data, and including first results from via fabrication.
- Month 29: Ten packaged devices delivered for evaluation by the US Government, developed on a sapphire substrate with ≥ 150 mm diameter and meeting the device temperature specifications.
- Month 30: Final report documenting yield, process development, transistor characterization, and a path to future voltage scaling while maintaining high frequency performance.

e. Dual Use Applications (Phase III)

The developed mm-wave GaN-on-sapphire technology would enable many commercial and DoD/military applications. For example, the large high quality epi wafer will enable the implementation of wafer-scale millimeter-wave integrated circuits for W-band 90 GHz radar imaging array to observe obstacles hidden in the rain or fog to guide low altitude military aircrafts or ground vehicles. For commercial applications, the material and device technologies developed in this program would enable the production of low cost millimeter-wave transceiver integrated circuit products for high bandwidth multi-gigabit data communications such as in 5G or 6G wireless cellular phones and backhaul base stations.

The proposer is required to identify one or more potential applications and efforts for Phase III. The proposer is required to obtain funding support from either the private sector, a non-SBIR Government source, or both, to develop the prototype into a viable product or non-R&D service for sale in military or private sector markets. Phase III refers to work that derives from, extends, or completes an effort made under prior SBIR funding agreements, but is funded by sources other than this Program.

Each of the following types of activity constitutes Phase III work:
• Commercial application (including testing and evaluation of products, services or technologies for use in technical or weapons systems) of SBIR/STTR-funded R/R&D financed by non-Federal sources of capital.
• SBIR/STTR -derived products or services intended for use by the Federal Government, funded by non-SBIR/STTR sources of Federal funding.
• Continuation of R/R&D that has been competitively selected using peer review or merit-based selection procedures, funded by non-SBIR Federal funding sources.
• Work may be for products, production, services, R/R&D, or any such combination.

f. References

[1] S. Wienecke, B. Romanczyk, M. Guidry, H. Li, X. Zheng, E. Ahmadi, K. Hestroffer, L. Megalini, S. Keller, U. Mishra, "N-Polar Deep Recess MISHEMTs With Record 2.9 W/mm at 94 GHz,' IEEE Electron Device Letters, Vol. 37, No. 6, June 2016

[2] O. Koksaldi, J. Haller, H. Li, B. Romanczyk, M. Guidry, S. Wienecke, S. Keller, U. Mishra, "N-Polar GaN HEMTs Exhibiting Record Breakdown Voltage Over 2000V and Low Dynamic On-Resistance", IEEE Electron Device Letters, Vol. 39, No. 7, July 2018

[3] Via, G. D., "GaN Reliability–Where we are and where we need to go." CS ManTech 2014 (2014): 15-18

[4] A. M. Darwish, A. J. Bayba, H.A. Hung, "Thermal Resistance Calculation of AlGaN–GaN Devices, IEEE Transactions on Microwave Theory and Techniques, Vol. 52, No. 11, November 2004

g. Keywords

Wide bandgap transistor, N-polar GaN, GaN on sapphire, mmW transistor, W-band transistor, semiconductor power amplifier

III. SUBMISSION OF QUESTIONS

DARPA intends to use electronic mail for all correspondence regarding this SBO. Questions related to the technical aspect of the research objectives and awards specifically related to this SBO should be emailed to HR001120S0019@darpa.mil. Please reference BAA HR001120S0019-11 in the subject line. All questions must be in English and must include the name, email address, and the telephone number of a point of contact.

DARPA will attempt to answer questions in a timely manner; however, questions submitted within seven (7) calendar days of the proposal due date listed herein may not be answered. DARPA will post a consolidated Frequently Asked Questions (FAQ) document. To access the posting please visit: http://www.darpa.mil/work-with-us/opportunities. Under the HR001120S0019-11 summary, there will be a link to the FAQ. The FAQ will be updated on an ongoing basis until one week prior to the proposal due date.

In addition to the FAQ specific to this SBO, proposers should also review the SBIR/STTR General FAQ list at: http://www.darpa.mil/work-with-us/opportunities?tFilter=&oFilter=29934. Under the HR001120S0019 summary, there is a link to the general FAQ.

Technical support for the Defense SBIR/STTR Innovation Portal (DSIP) is available Monday through Friday, 9:00 a.m. – 5:00 p.m. ET. Requests for technical support must be emailed to DoDSBIRSupport@reisystems.com with a copy to HR001120S0019@darpa.mil.