Small Business Innovation Research (SBIR) and
Small Business Technology Transfer (STTR)
Opportunity Announcement
HR001120S0019-03
PiezoMEMS PDK

Which program will fund this topic?
SBIR
What type of proposals will be accepted?
Both Phase I and Direct to Phase II (DP2)

Technology Area(s): Materials/Processes
DARPA Program: SHRIMP and FFE

I. INTRODUCTION

The Defense Advanced Research Projects Agency (DARPA) Small Business Programs Office (SBPO) is issuing an SBIR/STTR Opportunity (SBO) inviting submissions of innovative research concepts in the technical domain(s) of Materials/Processes. In particular, DARPA is interested in understanding the feasibility of a standardized PiezoMEMS process that can support a broadly useful process design kit (PDK).

This SBO is issued under the Broad Agency Announcement (BAA) for SBIR/STTR, HR001120S0019. All proposals in response to the technical area(s) described herein will be submitted in accordance with the instructions provided under HR001120S0019, found here: https://beta.sam.gov/opp/b8abeb02f16a4450b2c2f859fc00c177/view.

a. Eligibility

The eligibility requirements for the SBIR/STTR programs are unique and do not correspond to those of other small business programs. Please refer to Section 3.1, Eligible Applicants, of HR001120S0019 for full eligibility requirements.

b. Anticipated Structure/Award Information

Please refer to Section 1, Funding Opportunity Description provided in HR001120S0019 for detailed information regarding SBIR/STTR phase structure and flexibility.

If a proposer can provide adequate documentation to substantiate that the scientific and technical merit and feasibility described in the Phase I section of the topic has been met and describes the potential commercial applications, the Direct to Phase II (DP2) authority allows the Department of Defense (DoD) to make an award to a small business concern under Phase II of the SBIR program without regard to whether the small business concern was provided an award under Phase I of an SBIR program. This SBO is accepting both Phase I and DP2 proposal submissions.

For this SBO, DARPA will accept Phase I proposals for cost of up to $225,000 for a 9-month period of performance.

DARPA will accept DP2 proposals for cost of up to $1,750,000. This includes a 24 month base period not to exceed a cost of $1,000,000 and a 12 month option period not to exceed a cost of $500,000. A separately priced option of up to $250,000 must also be proposed for contractors who would like to be considered for participation in the DARPA Entrepreneurial Investigator Initiative. Refer to Section 2.6, DARPA Embedded Entrepreneur Initiative, of HR001120S0019 for detailed information on EEI.

Proposers should refer to Section 4, Application and Submission Information, of HR001120S0019 for detailed proposal preparation instructions. Proposals that do not comply with the requirements detailed in HR001120S0019 and the research objectives of this SBO are considered non-conforming and therefore are not evaluated nor considered for award.

Phase I proposals shall not exceed 20 pages. Phase I commercialization strategy shall not exceed 5 pages. This should be the last section of the Technical Volume and will not count against the 20-page limit. Please refer to Appendix A of HR001120S0019 for detailed instructions on Phase I proposal preparation.

DP2 Feasibility Documentation shall not exceed 40 pages. DP2 Technical Proposal shall not exceed 40 pages. Phase II commercialization strategy shall not exceed 5 pages. It should be the last section of the Technical Volume and will not count against the 40-page limit. Please refer to Appendix B of HR001120S0019 for detailed instructions on DP2 proposal preparation.

c. Evaluation of Proposals

Section 5, Evaluation of Proposals, in HR001120S0019 provides detailed information on proposal evaluation and the selection process for this SBO.

d. Due Date/Time

Full proposal packages (Proposal Cover Sheet, Technical Volume, Price/Cost Volume inclusive of supporting documentation, and Company Commercialization Report) must be submitted via the DoD SBIR/STTR Proposal Submission website per the instructions outlined in HR001120S0019 no later than **2:00 pm ET, April 20, 2020.**

II. TOPIC OVERVIEW

a. Objective

Develop a piezoelectric MEMS process and supporting generalized process design kit (PDK), capable of accepting a wide range of conventional substrates (e.g. Si, Si on insulator (SOI), cavity-SOI, sapphire), allowing DoD prototyping and low volume production of state-of-the art piezoelectric MEMS components.

b. Description

One of the most commercially successful MEMS devices in the last two decades has been resonators and filters based on piezoelectric AlN thin films. Specifically, both film bulk

acoustic resonators (FBAR) [1] and solidly mounted resonators (SMR) [2] revolutionized the wireless communication industry with a low profile, low cost filter technology covering frequencies ranging from MHz to low GHz. Despite the successes in FBAR and SMRs for the wireless industry, there are essentially no options for DoD access to AlN based MEMS fabrication capabilities for custom devices required for DoD systems. Furthermore, global interest in piezoelectric MEMS (PiezoMEMS) including both AlN and lead zirconate titanate (PZT) based MEMS has been expanding, including recent press releases announcing AlN device processing and integration on 200mm diameter CMOS wafers [3]. Much of this global interest is focused on FBAR and SMR but also expanding into piezoelectric micromachined ultrasonic transducers (pMUT), acoustic sensors (e.g. microphones), and solid-state transducers (e.g. finger print sensors) to name a few [4, 5].

To take advantage of these growing capabilities, DoD researcher and developer access to commercial quality PiezoMEMS fabrication processes is paramount. Beyond simple access to AlN and other PiezoMEMS based manufacturing capabilities, another significant challenge is the lack of a generalized process design kit (PDK) for MEMS devices. Unlike the integrated circuit community, the MEMS community has found it difficult to develop generalized PDKs for its more mature processes because process and design rules tend to be design specific, and PDK generalization has been limited by a low number of product designs manufactured at each manufacturer.

To address these concerns, DARPA is interested in developing a substrate agnostic PiezoMEMS fabrication process capable of accepting a wide range of conventional substrates (e.g. Si, Si on insulator (SOI), cavity-SOI, sapphire), along with a supporting PDK that is generalized to the fabrication process and not limited to a single device type. As an example, this PiezoMEMS process could consist of two modules, one for the PiezoLayers and one for the PiezoRelease. A notional example of the PiezoLayer module is illustrated in Figure 1 to highlight the substrate agnostic objective. Additional interlayer dielectric layers and/or metallization layers may be expected as part of either the notional PiezoLayer or PiezoRelease module. The proposed approach will develop a generalized PDK covering material properties, processing parameters, example device simulated and experimental data appropriate for use by novice designers and incorporating a range of device parameters (thickness, composition, etc.) which is relatively substrate agnostic. The proposed effort must additionally demonstrate a standard of reproducibility with minimal variation on key material and processing parameters thereby minimizing the resulting device variations.

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[1] https://www.broadcom.com/products/wireless/fbar
[2] https://www.qorvo.com/applications/mobile-products/advanced-filter-solutions
[3] https://www.memsjournal.com/2018/06/mems-foundry-silterra-unveils-monolithic-pmut-on-cmos-platform.html
[4] R. Aigner, "BAW Filters and Duplexers for Mobile Communication," *Piezoelectric MEMS Resonators*, eds (Bhugra and Piazza, Springer, 2017, pp 387-413.
[5] I. Kanno, "Piezoelectric MEMS: Ferroelectric Thin Films for MEMS Applications," Jpn. J. Appl. Phys, 57, 040101, 2018.

The PDK design document should, at a minimum, contain information on the following details:

- Material property data for the piezoelectric, metal, and other layers that will be made available within the process flow
- Process design rules to include but not limited to layer thicknesses, critical dimensions, and offset dimensions
- Processing control data for each processing step
- Design rule checking capability
- Material property and process control test structures
- Supporting process control monitoring data to illustrate process reproducibility
- Example device simulations and experimental data to illustrate the process
- Example design models are also desired for the PDK design document, though not mandatory.

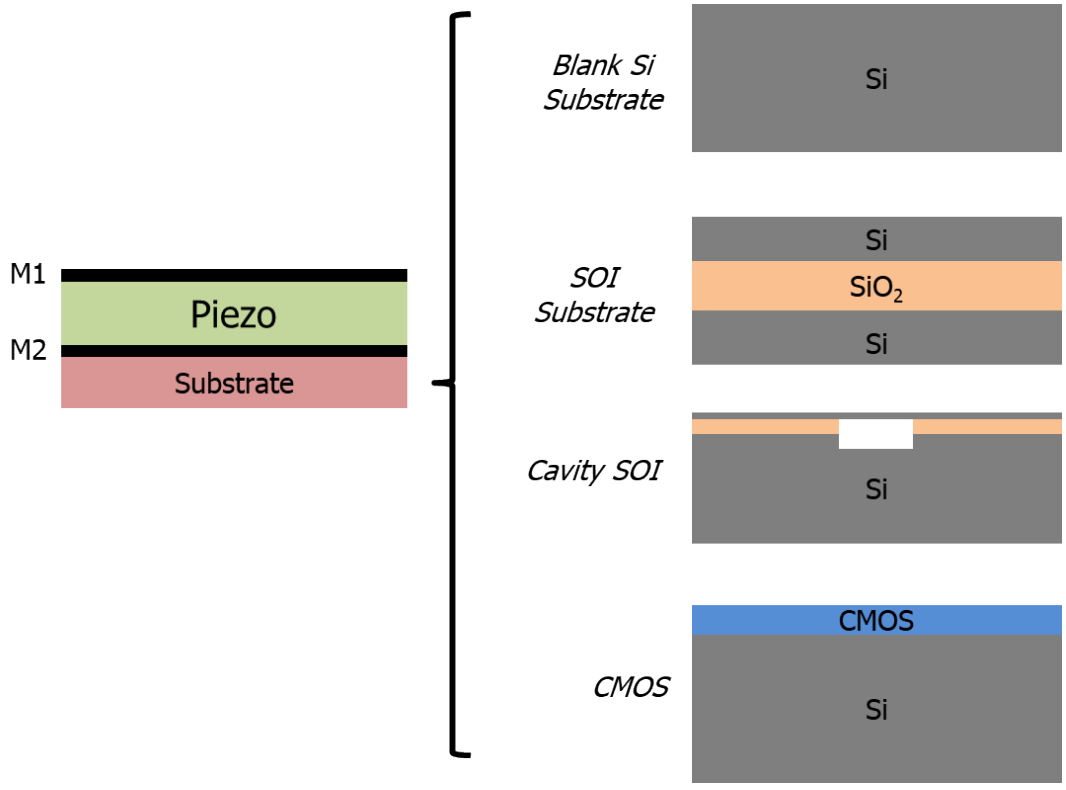

Figure 1: Illustration of a notional PiezoLayer Module consisting of a bottom electrode (M2), a piezoelectric layer (Piezo), and a top electrode (M1) capable of being implemented on a variety of substrates.

c. Phase I (9 months)

Phase I efforts will focus on the development of a piezoelectric MEMS process suitable for integration in a commercial microelectronic integrated circuit process flow. The process should be suitable for deposition on a range of commercially relevant substrates (e.g. Si, Si on insulator (SOI), cavity-SOI, sapphire), and should fall within a range of material property and process metrics, which should be repeatedly achieved against a maximum variance. The final process should be suitable for low volume prototyping and at a sufficiently advanced state to have a basic PDK created for potential future designers. Proposals should not only include specifics about the process but also how material, process, and test structures will be evaluated.

Proposers interested in submitting a Direct to Phase II (DP2) proposal must include a detailed description and demonstrated data within their feasibility documentation that demonstrates the achievement of all metrics listed in the Phase 1 metrics table. For detailed information on DP2 requirements and eligibility, please refer to Section 4.2, Direct to Phase II (DP2) Requirements, and Appendix B of HR001120S0019

i. Metrics

Program success will be based on achieving the metrics listed in the table below. All parameters are expected to be measured over a reasonable sample size and *proposals should indicate the sample size (larger sizes are desirable).*

PDK	Parameter	Metric Range	Notes
Process	Number of Substrate Types	>= 3	Standard deposition substrates
	Substrate size	150 – 300 mm	
	Cross Wafer Composition Variance	+/-2%	
	Wafer-to-Wafer Composition Variance	+/- 2%	
	Piezoelectric layer thickness range	0.5 to 1.0 µm	<3% variance cross wafer, wafer-to-wafer
	Smallest electrode dimension	<=2 µm	
	Largest electrode dimension	>= 1.0 mm	
	Minimum spacing	<=10 µm	
	Sidewall Angle	> 50°	
	Piezoelectric etch loading factor	> 80%	
Material Properties (at room temperature)	Piezoelectric layer crystal orientation	(001) for PZT (0002) for AlN	
	Piezoelectric layer phase purity (e.g. Lotgering factor)	> 90 % (median across wafer)	

	Piezoelectric coefficient ($e_{31,f}$)	< -1 C/m^2 (median across wafer)	
	Dielectric constant (ε_{33})	10 - 2000 (median across wafer)	
	Piezoelectric crystal grain size	User defined, polycrystalline, single crystal	
	Young's modulus	> 50 MPa	
	Residual stress range (average value per layer)	+/- 500 MPa	- Measure individual layers and the entire PiezoLayer stack - Individual layer variance across wafer and wafer-to-wafer → +/- 50 MPa
Release Module and Other Features	Release etch, timed, undercut tolerance	<=8 µm	Only one release etch variant is required in Phase 1
	Release etch, defined (e.g. cavity SOI)	<=5 µm	
	Trimming steps (e.g. frequency, capacitance, etc.)	>= 0	Wafer level capability
User Device	User defined device metrics (e.g. resonator k_t^2, quality factor, tuning range)	User Defined	

ii. Schedule/Milestones/Deliverables

- Month 1: Kickoff meeting detailing initial approaches
- Month 3: Verification of all material parameters
- Month 6: Verification of processing parameters
- Month 9: Demonstration of example structures and baseline PDK

d. Phase II (24 months)

Phase II efforts will focus on refinement of the MEMS process and concentrate on the development of the full PDK. The final PDK should not require updating of the process flow or PDK based on the choice of substrate, piezoelectric layer thickness, or doping level of the piezoelectric material. As an example, this feature will provide flexibility in frequency, kt2, and Q and enable rapid uptake of the latest material developments into this process and PDK. The final PDK will leverage commercial fabrication techniques to reduce costs and keep DoD processes up to date with the latest technology/fabrication/materials developments.

i. Metrics

Program success will be based on achieving the metrics listed in the table below. All parameters are expected to be measured over a reasonable sample size and *proposals should indicate the sample size (larger sizes are desirable).*

PDK	Parameter	Metric Range	Notes
Process	Number of Substrate Types	>= 4	Standard deposition substrates
	Substrate size	150 – 300 mm	
	Cross Wafer Composition Variance	+/-2%	
	Wafer-to-Wafer Composition Variance	+/- 2%	
	Additives/dopant range	> 5%	e.g. Sc doping in $Al_xSc_{1-x}N$
	Piezoelectric layer thickness range	0.1 to 1.5 µm	<3% variance cross wafer, wafer-to-wafer
	Smallest electrode dimension	<=2 µm	
	Largest electrode dimension	>= 1.0 mm	
	Minimum spacing	<=5 µm	
	PiezoLayer sidewall angle	> 70°	
	Piezoelectric etch loading factor	> 80%	
	Process feature reproducibility (sidewall angle, thickness, etc.)	<= 5%	
Material Properties (at room temperature)	Piezoelectric crystal quality (e.g. Lotgering factor)	> 90 % (median across wafer)	
	Piezoelectric coefficient ($e_{31,f}$)	< -1 C/m^2 (median across wafer)	
	Dielectric constant (ε_{33})	10-2000 (median across wafer)	
	Piezoelectric crystal grain size	User defined, polycrystalline, single crystal	
	Young's modulus	> 50 MPa	
	Residual stress range (average value per layer)	+/- 500 MPa	- Measure individual layers and the entire PiezoLayer stack - Individual layer variance across wafer and wafer-to-wafer → +/- 50 MPa
	Material layer reproducibility	<= 3%	

Release Module and Other Features	Release etch, timed, undercut tolerance	<=4 μm	
	Release etch, defined (e.g. cavity SOI)	<=2 μm	
	Trimming steps (e.g. frequency, capacitance, etc.)	>= 1	Wafer level capability
	Design rule checking accuracy	> 95%	
User Device	User defined device metrics (e.g. resonator k_t^2, quality factor, tuning range)	User Defined	

ii. Schedule/Milestones/Deliverables

- Month 1: Kickoff meeting detailing initial approaches
- Month 6: Technical reports detailing PDK maturity and progress towards milestones
- Month 12: Early PDK suitable for use by expert designers, demonstration of material and processing metrics, demonstration of user defined device metrics within 80% of defined goals, sample wafers (quantity of 1 with only the piezoelectric layer) and devices (quantity of 3 of each type) for independent verification
- Month 18: Technical reports detailing PDK maturity, design rule checking, and progress towards milestones
- Month 24: Final technical report detailing final PDK at 24 months suitable for use by novice designers, demonstration of material and processing metrics, demonstration of user defined device metrics within 95% of defined goals, sample wafers (quantity of 3 with only the piezoelectric layer) and devices (quantity of 5 of each type) for independent verification

Phase II Option (12 months)

The Phase II option will include submission by outside designers into the relevant process using the developed PDK. Towards this, proposers will need to:

- Identify and include 2-3 external designers from industry, academic, or government groups
- Offer 2 multi-project wafer (MPW) runs on the relevant process flow using the proposed PDK
- Report detailing updated PDK, demonstration of material and processing metrics from each of the MPW runs, and demonstration of user defined device metrics within 95% of defined goals

e. Dual Use Applications (Phase III)

Potential DoD/military applications for this technology include filters for tactical radios and electronic warfare systems and acoustic sensors for unattended ground sensors. Potential commercial uses of substrate agnostic, PiezoMEMS fabrication process and PDK include IF and RF filters, ultrasonic transducers, acoustic sensors, solid-state transducers, oscillators, memory and computing.

f. References

1. https://www.broadcom.com/products/wireless/fbar
2. https://www.qorvo.com/applications/mobile-products/advanced-filter-solutions
3. https://www.memsjournal.com/2018/06/mems-foundry-silterra-unveils-monolithic-pmut-on-cmos-platform.html
4. R. Aigner, "BAW Filters and Duplexers for Mobile Communication," Piezoelectric MEMS Resonators, eds (Bhugra and Piazza, Springer, 2017, pp 387-413.
5. Kanno, "Piezoelectric MEMS: Ferroelectric Thin Films for MEMS Applications," Jpn. J. Appl. Phys, 57, 040101, 2018.

g. Keywords

MEMS, AlN, AlScN, PiezoMEMS, piezoelectric, Process Design Kit, Manufacturing, PDK, PZT, lead zirconate titanate

III. SUBMISSION OF QUESTIONS

DARPA intends to use electronic mail for all correspondence regarding this SBO. Questions related to the technical aspect of the research objectives and awards specifically related to this SBO should be emailed to HR001120S0019@darpa.mil. Please reference BAA HR001120S0019-03 in the subject line. All questions must be in English and must include the name, email address, and the telephone number of a point of contact.

DARPA will attempt to answer questions in a timely manner; however, questions submitted within seven (7) calendar days of the proposal due date listed herein may not be answered. DARPA will post a consolidated Frequently Asked Questions (FAQ) document. To access the posting please visit: http://www.darpa.mil/work-with-us/opportunities. Under the HR001120S0019-03 summary, there will be a link to the FAQ. The FAQ will be updated on an ongoing basis until one week prior to the proposal due date.

In addition to the FAQ specific to this SBO, proposers should also review the SBIR/STTR General FAQ list at: http://www.darpa.mil/work-with-us/opportunities?tFilter=&oFilter=29934. Under the HR001120S0019 summary, there is a link to the general FAQ.

Technical support for the Defense SBIR/STTR Innovation Portal (DSIP) is available Monday through Friday, 9:00 a.m. – 5:00 p.m. ET. Requests for technical support must be emailed to DoDSBIRSupport@reisystems.com with a copy to HR001120S0019@darpa.mil.