What is the Electronics Resurgence Initiative?

Defense Industry Executive Summit

July 11, 2017
Program managers from the community...

on a temporary 3 to 5 year assignment...

executing ~$3 billion in the hands of ~90 PM's through ~250 programs...

to eliminate technical surprise.

How do we operate?

Programs / Challenges

Commercial Impact

National Defense Needs
DARPA has evolved to using challenges

2005

2015

Today

2020

Grand Challenge
(2005-2007)
2014 2015 2016 2017

2015

Robotics Challenge

Video not included

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2016

Cyber Grand Challenge

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Exploring the capabilities of learning / autonomy and their societal impact

Grand Challenge (2005-2007)

Robotics Challenge (2012-2015)

Cyber Grand Challenge (2016)

Spectrum Collaboration Challenge (2017-2018)
But, we still have a long way to go

A revolution in sensing and processing is required
“...The complexity for minimum component costs has increased at a rate of roughly a factor of two per year (see graph)…”

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VIII. DAY OF RECKONING

Clearly, we will be able to build such component-crammed equipment. Next, we ask under what circumstances we should do it. The total cost of making a particular system function must be minimized. To do so, we could amortize the engineering over several identical items, or evolve flexible techniques for the engineering of large functions so that no disproportionate expense need be borne by a particular array. Perhaps newly devised design automation procedures could translate from logic diagram to technological realization without any special engineering.

It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.
Pseudolithic Integration

Specialized Hardware Blocks

Software Hardware Co-design

Compiler-directed Hardware
Reconfiguration
Sparse + Dense

3.0 µm

30.0 µm
Where are we heading?

Sowing the seeds for a revolution in processing
What is the initiative?

Program managers hired directly from the electronics community...

Aligning incentives as we both stare at an uncertain future

Co-developing electronics to manage the coming inflection to support both a national electronics base and national defense
MTO ELECTRONICS RESURGENCE INITIATIVE TIMELINE

Launch, Learn, & Organize
6/21: Industry Discussion
7/11: Defense Base Summit

Summer of Listening
7/18: 2-day workshop on Materials, Architectures, Designs

Open Competition
9/12: Proposals Requested (Expected)

Complete Contracting
4/20: Start Work

Happening Now
Summer 2017
Fall 2017
Spring 2018

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$75 Million Additional in FY18 Budget
Press Release Announcing Initiative
2025 - 2030

NATIONAL ELECTRONICS CAPABILITY

$216 MILLION TOTAL (FY18)

$141 million in Current Efforts (FY18)

$75 million Of New Funding (FY18)

materials architectures designs

JUMP + Traditional Programs

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Traditional Programs Currently Funded

- **JUMP** – Joint University Microelectronics Program
- **CHIPS** – Common Heterogeneous Integration and IP Reuse Strategies
- **HIVE** – Hierarchical Identify Verify Exploit
- **L2M** – Lifelong Learning Machines
- **SSITH** – System Security Integrated Through Hardware and software
- **N-ZERO** - Near-Zero Power Radio Frequency Receivers
- **CRAFT** – Circuit Realization at Faster Time Scales

**JUMP + Traditional Programs**

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Joint University Microelectronics Program (JUMP)

DARPA
Industry

40%
60%

Joint University Microelectronics Program (JUMP)

RF to THz Distributed Computing Cognitive Computing Intelligent Memory/Storage Advanced IC Architectures Devices/Materials

World Class Idea Generation

Stanford University
3D System on Chip

Linton Salmon
DARPA Program Manager

The intersection of industry, academics, and government

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National Electronics Capability

World Class Idea Generation

Stanford University 3D System on Chip

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Circuit Realization at Faster Time Scales (CRAFT)

Driving a design methodology that can be used to quickly design flexible, high performance custom integrated circuits using leading-edge CMOS technology while driving DoD to use the best commercial fabrication and design practices.

Sharply reduce barriers to DoD use of leading-edge custom integrated circuits (ICs) for orders-of-magnitude higher performance at low power for DoD systems.
Hierarchical identify Verify Exploit (HIVE)

Next-generation server processor designed to find patterns in streaming data sets by using graph analytics

Enabling the DoD to perform graph analytics at the edge of the battlefield and not rely on datacenters back in the United States; providing greater situational awareness in addition to the ability to do real time sensor fusion and exploitation at the lowest echelons.
Lifelong Learning Machines (L2M)

Pursuing approaches for biologically-inspired artificial intelligence utilizing flexible models to continue adapting during execution in the field

Fundamentally new machine learning mechanisms for machines that learn continuously as they operate
Secure Processing Architecture by Design (SPADE)

Incorporating untrusted commercial devices with proprietary trusted government designs

Technology-driven security techniques can enable new DoD options for acquiring state-of-the-art, commercial microelectronics
Common Heterogeneous Integration and IP Reuse Strategies (CHIPS)

Developing the design tools and integration standards required to demonstrate modular integrated circuit (IC) designs that leverage the best of the DoD and commercial designs and technology.

CHIPS enables rapid integration of modular circuits at the die level.
System Security Integrated Through Hardware and software (SSI TH)

Develop hardware design tools to provide inherent security against hardware vulnerabilities exploited through software in DoD and commercial electronic systems.

Circuit design tools that can be used to implement security architectures in DoD and commercial integrated circuits.

Hardware protection
Flexible
Scalable
Integrated architecture

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How do we lower the design barrier to specialization?

Andreas Olofsson
Designs

From Kickstarter to Supercomputer
World’s first crowd-funded chip

2012 Parallella Kickstarter

16-core 65nm Processor (<2W)
System-on-chip design costs are inhibiting US innovation

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Design: The curse of Moore’s Law

- Automation
- Transistors

- 4004
- 8088
- 486
- Pentium4
- Westmere


10,000,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
1,000
100
10
1

0.00 0.10 0.20 0.30 0.40 0.50 0.60 0.70 0.80 0.90 1.00

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IP: Reuse and complexity growth

- 2016:
  - 175 IP blocks
  - 80% reuse

Average % of reused IP blocks

<table>
<thead>
<tr>
<th>Year</th>
<th>Average number of IP blocks</th>
<th>Percent of reuse</th>
</tr>
</thead>
<tbody>
<tr>
<td>1998</td>
<td>18 blocks</td>
<td>0%</td>
</tr>
<tr>
<td>1999</td>
<td>20 blocks</td>
<td>10%</td>
</tr>
<tr>
<td>2000</td>
<td>25 blocks</td>
<td>20%</td>
</tr>
<tr>
<td>2001</td>
<td>30 blocks</td>
<td>30%</td>
</tr>
<tr>
<td>2002</td>
<td>35 blocks</td>
<td>40%</td>
</tr>
<tr>
<td>2003</td>
<td>40 blocks</td>
<td>50%</td>
</tr>
<tr>
<td>2004</td>
<td>45 blocks</td>
<td>60%</td>
</tr>
<tr>
<td>2005</td>
<td>50 blocks</td>
<td>70%</td>
</tr>
<tr>
<td>2006</td>
<td>55 blocks</td>
<td>80%</td>
</tr>
<tr>
<td>2007</td>
<td>60 blocks</td>
<td>90%</td>
</tr>
<tr>
<td>2008</td>
<td>65 blocks</td>
<td>100%</td>
</tr>
<tr>
<td>2009</td>
<td>70 blocks</td>
<td></td>
</tr>
<tr>
<td>2010</td>
<td>75 blocks</td>
<td></td>
</tr>
<tr>
<td>2011</td>
<td>80 blocks</td>
<td></td>
</tr>
<tr>
<td>2012</td>
<td>85 blocks</td>
<td></td>
</tr>
<tr>
<td>2013</td>
<td>90 blocks</td>
<td></td>
</tr>
<tr>
<td>2014*</td>
<td>95 blocks</td>
<td></td>
</tr>
<tr>
<td>2015*</td>
<td>100 blocks</td>
<td></td>
</tr>
<tr>
<td>2016*</td>
<td>105 blocks</td>
<td></td>
</tr>
<tr>
<td>2017*</td>
<td>110 blocks</td>
<td></td>
</tr>
<tr>
<td>2018*</td>
<td>115 blocks</td>
<td></td>
</tr>
<tr>
<td>2019*</td>
<td>120 blocks</td>
<td></td>
</tr>
</tbody>
</table>

Average # of IP blocks: 250

- 1998: 20 blocks
- 1999: 25 blocks
- 2000: 30 blocks
- 2001: 35 blocks
- 2002: 40 blocks
- 2003: 45 blocks
- 2004: 50 blocks
- 2005: 55 blocks
- 2006: 60 blocks
- 2007: 65 blocks
- 2008: 70 blocks
- 2009: 75 blocks
- 2010: 80 blocks
- 2011: 85 blocks
- 2012: 90 blocks
- 2013: 95 blocks
- 2014: 100 blocks
- 2015: 105 blocks
- 2016: 110 blocks
- 2017: 115 blocks
- 2018: 120 blocks

Research Corporation, 2014

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Verification: “Software is eating the world”

5-10K Lines of Control Code

>100K Lines of Application S/W

Video Display

20-50K Lines of Protocol F/W

Wireless

250-500K Lines of F/W

250-300K Lines of DSP F/W

TV Decode

50-100K Lines of Protocol F/W

Over 2M Lines of Application S/W

xDSL

Up to 2M Lines of Network S/W

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Masks: Expensive but manageable

The total cost of producing 10,000 units of an “Apple-A9” grade 14nm custom SoCs is only $1.8M!
How do we get out of the SoC tar pit?
COTS FPGAs are great, but not appropriate for every application!

Source: Multiple industry market trackers & DMEA internal data from FPGA manufacturers

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Sprouts of hope...

Apple A10 SoC

<table>
<thead>
<tr>
<th>Process</th>
<th>TSMC 16FF+</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistors</td>
<td>3.3B</td>
</tr>
<tr>
<td>Die Area</td>
<td>117 mm²</td>
</tr>
</tbody>
</table>

1024-core 64-bit Microprocessor

<table>
<thead>
<tr>
<th>Process</th>
<th>TSMC 16FF+</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistors</td>
<td>4.5B</td>
</tr>
<tr>
<td>Die Area</td>
<td>117 mm²</td>
</tr>
<tr>
<td>Performance</td>
<td>2 TFLOPS</td>
</tr>
<tr>
<td>RTL to GDS</td>
<td>~24hrs</td>
</tr>
<tr>
<td>Engineers</td>
<td>1</td>
</tr>
</tbody>
</table>

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My Questions
Can DARPA help industry get over the design cost hump?

Chip costs (design + production)

- Industry Total Cost
- DoD Total Cost
- Industry Production Cost
- DoD Production Cost

Status Quo

100% Automation
2X silicon Area

100% Automation
1X silicon Area

IDEA research year

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.
Can we leverage best practices from other industries?

<table>
<thead>
<tr>
<th>Industry</th>
<th>Average Lines of Code</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>AVERAGE LUXURY AUTO</strong></td>
<td>100M</td>
</tr>
<tr>
<td><strong>NAVIGATION SYSTEM IN 2009 S-CLASS MERCEDES-BENZ</strong></td>
<td>20M</td>
</tr>
<tr>
<td><strong>AVERAGE 2010 FORD AUTO</strong></td>
<td>10M</td>
</tr>
<tr>
<td><strong>BOEING 787 DREAMLINER</strong></td>
<td>6.5M</td>
</tr>
<tr>
<td><strong>U.S. AIR FORCE F-35 JOINT STRIKE FIGHTER</strong></td>
<td>5.7M</td>
</tr>
<tr>
<td><strong>U.S. AIR FORCE F-22 RAPTOR JET</strong></td>
<td>1.7M</td>
</tr>
</tbody>
</table>

**Lines of Software Code in Ford Vehicles (Millions)**

- **2005**: 2.4M
- **2009**: 6M
- **2010**: 10M

Sources: IEEE; Automotive Designline

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Should we pursue an open-source strategy?

Facebook Market Cap: $433B!

User Content

Facebook Code

- MemCache
- MySQL
- Yoga
- Thrift
- Apache
- PHP
- Cassandra
- Jenkins
- ...

LINUX

$15B+ Open source codebase

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Can we automate “all of it”? 

- Machine generated chip and package layout
- Machine generated board layout
- Intent driven system generation
Can we design by intent?

**Memory:**
- 1GB DDR3
- 128MB Flash

**Processor:**
- 2 x ARM-A9
- FPGA
- 20 GFLOPS

**Interface:**
- 5V,
- Ethernet,
- USB,
- HDMI, 5V

**Power:**
- 5V in:
  - 1.8V
  - 2.5V
  - 3.3V out

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Can we reinvent SiP and PCB design?

**Today**
- **Manual Part Selection**
- **Manual Schematic**
- **Manual Layout**

- 100% Manual
- Error prone
- Rarely optimal

**Future**
- **Intent**
- **System Generator**
- **Schematics**
- **Pruning**
- **Goal Optimizer**
- **New Concept**: Machine synthesized board from intent and open COTS parts library.

**Potential Solutions**
- Inexact Description
- Open Parts DB

**Goal**
- Optimizer
- Schematic
- Layout Generator
Can we fully automate analog layout?

Today
Designer provides manual constraints to layout person (or tool)

Max 10μm from main supply, 0.5μm width

Common centroid layout

Place dummies, interdigitize

Future

Circuit Classifier
Assign Strategies
Auto-Placement
Auto-Routing

Common Vocabulary of Strategies

Centroid
Mirroring
Isolation

Common terms:
VDD
IBIAS
VSS
VIN
VIP
VOUT

Model
Training

Isolate with guard ring and well!

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Can we augment design teams with machine learning?

**Today**
- Improved power, performance, area possible with custom datapaths
- Not possible in existing EDA solutions without significant manual work

**Future**
- Automatic datapath circuit classification
- Circuit specific cost models
- Multi-strategy digital placers

Leverage graph pattern asymmetries

Significant wire length improvement

[Pan, UT Austin]
Will modern SoC design ever look like this?

- Easy and fun
- Black box encapsulation
- Robust and simple plug and play interfaces
My DARPA dream...

...when I leave DARPA...

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How do we integrate new materials for specialized functions?

Dan Green / Linton Salmon

Steering the science of materials to commercial product lines

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.
300mm diameter Si CMOS wafer

Si (45nm), InP (TF5 HBT), GaN (GaN20 HEMT)
Three-dimensional crossbar arrays of self-rectifying Si/SiO$_2$/Si memristors

Can Li, Li-Hao Hsu, Hsin-Jung Hsing, Yao-Hung Jeng, Ping Lin, Qiu-Mei, Mark Barnett, J. Joshua Yang, Hustin L. Lin & Jonghee Ha

Nature Communications 8, Article number: 19668 (2017)
DOI:10.1038/ncomms19668
Received: 21 October 2016
Accepted: 19 April 2017
Published online: 05 June 2017

Three-dimensional integration of nanotechnologies for computing and data storage on a single chip

Max M. Shulaker, Gage Hult, Rebecca S. Park, Roger T. Howe, Krishna Srinivasu, H.-S. Philip Wong & Subhasish Mitra

Nature 467, 74-78 (06 July 2017) | doi:10.1038/nature22364
Received 15 August 2016 | Accepted 02 May 2017 | Published online 05 July 2017

Analog signal and image processing with large memristor crossbars

Can Li, Miao Hsu, Yunning Liu, Hao Jiang, Ning Ge, Eric Montgomery, Norma D’Avila, Catherine E. Graves, Zhiyong Li, John Paul Strachan*, Peng Lin, Wenhao Song, Zhongrui Wang, Mark Barnett, Qing Wu, R. Stanley Williams, J. Joshua Yang*, Qiangfei Xia *

*Department of Electrical and Computer Engineering.

University of Massachusetts, Amherst
Stanford University
University of California, Santa Barbara
How do we manage the complexity of specialization with new architectures?
GNU Radio

Tom Rondeau
Architectures
The intersection of connectivity and computation

Wade Shen
Architectures
The intersection of big data and architecture
General Purpose Processor
Portable and programmable

Programmable Logic
Concurrent stream processing

Graphics Processing Unit
Embarrassingly Parallel

Digital Signal Processor
Optimized serial processing

Accelerator
The best at one thing

Math Domains
- Dense Linear Algebra
- Transforms
- Learning, optimization

Performance
- Power
- Bandwidth
- Latency

Programming Tools
- Compilers
- Debuggers
- Performance measurements/tools

Data Representation
- Data Structures
- Fixed point math
- Numerical precision / quantization

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How do we integrate new materials for specialized functions?

How do we manage the complexity of specialization with new architectures?

How do we lower the design barrier to specialization?
The backdrop to this initiative

Commercial involvement around the world
The headlines are focused on China:

- U.S. Semiconductor Sector Faces Risk From China, Says White House Report
- China Bets on Sensitive U.S. Start-Ups, Worrying the Pentagon
- Concern Grows in U.S. Over China's Drive to Make Chips
- Plan for $10 Billion Chip Plant Shows China's Growing Pull

The United States has notable advantages:

- Top 3 fabless companies ★
- Top 3 electronic design automation companies ★
- Two of the top 3 equipment manufacturers ★
- Top integrated device manufacturer ★
- Three of the 5 leading-edge foundries ★

U.S.-headquartered firms account for half of global semiconductor sales

1 2017 PCAST report “Ensuring Long-Term U.S. Leadership in Semiconductors”

Although the U.S. electronics advantage is not without challenges, we have the edge in microelectronics

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ARM in China joint venture to help foster 'secure' chip technology

UK chip designer says work to do to prevent sensitive leaks to rogue states

CHENG TING-FANG and DEBBY WU, Nikkei staff writers

TAIPEI – ARM Holdings, a British chip innovator controlled by SoftBank Group, will form a joint venture with Chinese partners "within months" to help companies in China develop semiconductor technologies, including products that could have security uses, a company executive told the Nikkei Asian Review on Monday.
Models for engagement?
An introduction to current corporate engagements at DARPA
Defense and National Needs

(HIVE)  (CRAFT)  (Possible)

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MTO has started new partnerships with the commercial sector in areas of shared interest.

- Northrop Grumman
- Pacific Northwest National Laboratory
- Georgia Tech
- Intel
- Qualcomm
Intel and DARPA: HIVE for Graph Analytics

Josh Fryman, PhD, Senior Principal Engineer
PI for Intel’s DARPA HIVE program

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.
Graph Analytics: DARPA’s “Big Bet”

• Thought leaders in academia, gov’t, industry believe that unstructured data will be encoded into sparse matrices and analyzed
  • The world is inherently sparse, not dense
  • Stages of processing and compute types alternate
  • Emerging future opportunities, insights

• DARPA HIVE is a proposal to build a Graph Analytics Processor
  • Goal: 1,000x superior GTEPS processing “efficiency”
    • GTEPS = Giga-TEPS = Traversed Edges per Second
  • Existing workloads and state-of-the-art to be used as baseline
The Challenges

Processor Design
- Optimized for dense math and cache use
- ~96% of time is spent moving data

Memory System
- Graph problems driven by “random accesses”
- Parallel memory access enables random access

Interconnect Design
- Scale poorly for data movement problems
- Scalable interconnect Balance energy/execution time consumed in data transfer

Sparse Matrix data format/operations more efficient processing

Credit: Trung Tran, DARPA

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HIVE Organization

• Pros:
  • No ITAR
  • No security clearances
  • No single solution
  • Bootstrap ecosystem

• Cons:
  • Borders are “fuzzy”
  • Baseline opaque
  • Lines may not be good

• Benefit is worth risk
Research vs. Product

• Intel doesn’t do “design for hire”
  • Challenges must align with one of
    • Product Plans
    • Emerging opportunities
    • Risk reduction in solutions

• Product teams must be cautious
  • Massive (legacy) ecosystem
  • Cannot break things

• IP protections paramount
  • World-wide ongoing concerns

• Research needs to push edges
  • Challenges are dynamic
    • Emerging threads
    • Risk-reward scenarios
    • May not succeed

• R&D has to be aggressive
  • Add risk to cautious plans
  • Success maps to product quickly

• Contract structure critical
  • IP terms at critical “cost-share” %
Industry – Government: Both Can Align

• Commercial workloads abound
  • PageRank / Search
  • Cyber Attack Recognition
  • Medical records
  • Genomics / cancer
  • Financial / fraud
  • Natural language processing
  • Associative memories / AI
  • Predictive failures and responses
  • Many-to-Many, not 1:1 or 1:n

• Government concerns map
  • Same
  • Same
  • Same – for military medical needs
  • Similar – general pattern matching
  • Same – for procurement/contracts
  • Same
  • Same
  • Same
  • Same

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MTO has started new partnerships with the commercial sector in areas of shared interest.

75% Reduction in DoD Product Cycle Time

Defense, university, and commercial sectors working side-by-side towards a common goal.
NVIDIA’s DARPA Programs

- Ubiquitous High-Performance Computing (UHPC) - 2010-2012
- Power Efficiency Revolution for Embedded Computing Technologies (PERFECT) - 2012-2015
- VirtualEye - 2014-2017
- Circuit Realization at Faster Time Scale (CRAFT) - 2016-2018
Sample of NVIDIA PERFECT Technologies

Patch-based Image Processing Architectures

Low-voltage SRAM Assists
Reduced $V_{min}$: $0.75V \rightarrow 0.45V$

SRAM and Signaling Circuits

On-chip Charge Recycling Signaling
$<10fJ/bit-mm$

High-Performance Parallel Algorithms

CuFFT
Thrust
CUSPARSE
CUB
cuDNN
VirtualEye - An Offshoot of PERFECT
Demonstrate image processing capabilities enabled by PERFECT-era technologies

- Live Event: multiple cameras
  - Capture event with multiple (stereo) cameras
  - Reconstruct 3D structure in real-time
  - Stream to remote user
  - User selects virtual view

Vision
Real-time virtual views of events constructed using live input streams from multiple sensors, including mobile UAVs.

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Demonstrate image processing capabilities enabled by PERFECT-era technologies

Live Event: multiple cameras

Virtual View

Vision
Real-time virtual views of events constructed using live input streams from multiple sensors, including mobile UAVs.

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DARPA CRAFT Program
Circuit Realization at Faster Time Scale

CRAFT objectives
- Reduce custom IC design time by 10x and increase design robustness
- Reduce technology node migration effort by 80%
- Ensure high IP reuse for DoD systems

Approach
- Raise design abstraction level (hierarchy, generators, modern SW engineering)
- Automate front-end design flow, isolate process-specific design steps, and leverage common IP blocks ported across processes

Program structure
- Phase 1: 5 performers develop methodology and produce chips (MPW run)
- Phase 2: <5 performers (1) enable outsiders to test methodology, (2) port design
- Teams: industry/academic partnerships

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MATCH: Modular Approach To Circuits and Hardware

- Object-oriented HLS-based (OOHLS) Flow
  - C++/SystemC language for design
  - HLS tools automate pipelining, resource scheduling, FSM design
  - All communication through Latency-Insensitive (LI) channels
- Developed MatchLib: OOHLS library of hardware components
- Developed a unified SystemC/C++ architecture modeling framework

NVIDIA Harvard
Partnership to demonstrate design flow
MATCH: Modular Approach To Circuits and Hardware

Scalable automated Modular FloorPlanner (MFP) based on total wire-length optimization

Correct-by-construction top-level timing with fine-grained Globally-Asynchronous-Locally-Synchronous (GALS) Clocking

NVIDIA

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NVIDIA’s Approach to Gov’t Partnerships

Gov’t and NVIDIA must be aligned on program objectives

Research must be aligned with technical/strategic direction of the company

Results must have the potential for transfer to NVIDIA product teams

Vehicle for direct collaboration with universities

Georgia Tech

The University of California, Berkeley

Harvard University

University of Pennsylvania

The University of Texas at Austin

The University of Utah

University of Virginia

Stanford University
MTO has started new partnerships with the commercial sector in areas of shared interest.

Beta release of design flow in October 2017

Circuit Realization At Faster Timescales (CRAFT)

Defense, university, and commercial sectors working side-by-side towards a common goal

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So how do you get involved?

Timeline and structure
MTO ELECTRONICS RESURGENCE INITIATIVE TIMELINE

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Fall 2017

Complete Contracting
4/20: Start Work
Spring 2018

7 months

May Jun Jul Aug Sep Oct Nov Dec Jan Apr

Defense Base Summit 2-day Workshop Proposals Requested Proposals Submitted Partners Selected Funding Released

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