Digital RF Battlespace Emulator (DRBE)

Emulating the Real World in Real Time

Proposers Day

Paul Tilghman, Program Manager

2/13/19
DRBE is a computing architecture program to support generation of a large-scale real-time virtual RF environment

Accurately emulating the RF environment is a difficult problem-space which challenges COTS electronics
- Such emulation requires compute which is high density, high throughput, and low latency
- Existing COTS electronics do not support the intersection of these needs

DRBE will:
1. Explore new and novel computing architectures, technologies, and methodologies necessary to achieve both low latency and high throughput computation
2. Assemble an “array” of these novel computing devices into an HPC
3. Integrate the HPC into a tool-suite and architecture which emulates the RF spectrum with high fidelity
Today: Impracticality of “road miles” in the AI-enabled military

Due to cost, system complexity, and limited availability of military ranges, the future testing, evaluation and training of military systems will increasingly take place in a completely virtual environments.

Real-world “road miles” for AI

DoD’s LVC capabilities do not extend to sensors, and leading communities like self-driving cars do it the “old fashioned way”

Source: waymo.com/ontheroad
https://www.rand.org/content/dam/rand/pubs/research_reports/RR1100/RR1105/RAND_RR1105.pdf
Grand Vision for Next Generation of RF Systems

AI bots train for 180 years / day to beat humans

Vision: Radar and EW systems “train” 24/7/365

DRBE will build a large-scale, completely virtual RF test range

Source: openAI
New Approach: Large Scale RF Emulation
A Completely Virtual EW Range

DRBE
Real-time High Performance Computer
Digitally Emulate RF Environment

Real EW Systems

Emulated EW Systems

Real Radar Systems

Emulated Radar Systems

DRBE will allow real EW and radar systems to be interact in real-time on a completely virtual test range.

Sources: Dell, Harris, www.turbosquid.com, Raytheon
Today's Capabilities and Limitations Testing RF at Scale

Largescale hardware in the loop emulation combines simulation scale with open-air fidelity

Sources: utah.edu, Dynetics
State of the Art in Digital Channel Emulation

RF Channel Emulators

- **Commercial Emulators**
- **DRBE’s Colosseum**
- **DRBE Objective**
- **DRBE Threshold**

**FIDELITY (AVG # PROPAGATION PATHS)** vs **SCALE (PORTS² * MHZ)**
Design goals

- Wireless fidelity only sufficient for communications
- 256 Ports (128 software defined radios)
- 80 MHz per channel
- Tunable: 10 MHz to 6GHz

- 64 Virtex-7 FPGAs (157 Tera-Ops/s)
- 88% DSP utilization

Colosseum pushes the limits of RF emulation achievable by COTS processing,
but lacks the scale and fidelity needed for radar & EW
1. **Propagation**
   Amplitude, time, phase accurate
   \[ O(N^2) \]

2. **Signal Interaction with Environment**
   Clutter and Multipath
   \[ O(N^2) \]

3. **Signal Interaction with Moving Platforms**
   Radar Cross Section, Doppler spread
   \[ O(P^2) \]

4. **Ambient Environment**
   Background transmitters and multi-static reflection
   \[ O(P^3) \]

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**Physical Environment**
Reflections of a transmission cause multiple delayed copies of a signal to be received

**Digitally Emulated Environment**
A Finite Impulse Response (FIR) filter is used to emulate the properties of each unique reflection

Latency:
\[ x[n] \rightarrow \delta_0 \rightarrow \delta_L \rightarrow y[n] \]

Amplitude Error:
\[ T \]

Amplitude:
\[ \delta_1, \delta_2 \]

Delay:
\[ \delta_L \]

Memory depth:
\[ 300 \text{ km maximum range: Memory depth} = 3300 \mu s \]

Distribution A -- Unlimited Public Release

Source: Lockheed Martin
### Need for Domain Specific RF Emulation Architectures

<table>
<thead>
<tr>
<th># Nodes</th>
<th>Link BW (GHz)</th>
<th># Links</th>
<th>I/O Rate (TB/sec)</th>
<th>Latency (us)</th>
<th>Total Compute (TFLOPs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>156</td>
<td>1.0</td>
<td>14,958</td>
<td>149.58</td>
<td>3.3 us</td>
<td>20,750</td>
</tr>
</tbody>
</table>

Traditional HPC compute nodes (CPUs, FPGAs, GPUs) fail to achieve all necessary DRBE requirements.

### Achievability of system requirements with an array of hardware accelerators

<table>
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<tr>
<th>DRBE Requirement</th>
<th>FLOPs</th>
<th>Memory</th>
<th>Memory Bandwidth</th>
<th>IO Bandwidth</th>
<th>Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU (Xeon E7-8894 v4)</td>
<td>133 TMACs</td>
<td>12.2 Gb</td>
<td>77 Tb/s</td>
<td>7.7 Tb/s</td>
<td>2.5 us</td>
</tr>
<tr>
<td>GPU (NVIDIA V100)</td>
<td>125 TFLOPS</td>
<td>128 Gb</td>
<td>7.2 Tb/s</td>
<td>2.4 Tb/s</td>
<td>330 us</td>
</tr>
<tr>
<td>FPGA (Xilinx VU13P)</td>
<td>2.3 TMACs</td>
<td>408 Mb</td>
<td>92 Tb/s</td>
<td>8.4 Tb/s</td>
<td>2 us</td>
</tr>
<tr>
<td>FPGA (Xilinx VU37P)</td>
<td>1.7 TMACs</td>
<td>64 Gb</td>
<td>3.7 Tb/s</td>
<td>6.4 Tb/s</td>
<td>2 us</td>
</tr>
</tbody>
</table>

Source: top500.org
Challenges – latency (non-exhaustive)

**Processing & Memory Architecture**

**Challenge:** Deep CPU pipelines and multi-level caching improve instruction throughput at the cost of latency

What architectures exploit the intrinsic parallelism and memory access patterns of the domain without compromising latency?

**Memory Access**

**Challenge:** Off-chip memory access is too slow for most challenging data accesses. Consistent read/write of the same memory locations ensures more time spent fetching data than computing

Over half of die area could conceivably be dedicated to memory. How can memory accesses be ameliorated and stratified according to their individual latency needs?

```
for signal_i, channel_i in signals, channels
    yi_t = convolve(signal_i, channel_i)
    buffer = buffer + yi_t
```
Challenges – Scaling (non-exhaustive)

Core Scaling

Challenge: Scaling up with discrete cores drives interconnect and latency bottlenecks.

Creating larger increasingly complex cores is very costly. Integration of a number of simpler cores yields better cost-point, but compromises bisection bandwidth and latency.

Can hybrid scaling strategies achieve the best of both worlds?

Network Topology

Challenge: All-to-all connection data sharing quickly makes the DRBE problem unachievable. Statically pruned interconnects limit system generality.

Can a combination of network topology and data-aware routing create an interconnect topology which minimizes required interconnect bandwidth?
The key technical challenge to DRBE is the intersection of high throughput, high density, low latency computing

Many issues exist which challenge traditional architectures

DARPA envisions no specific solution(s) to this problem space. And is open to any solution space that meets the BAA criteria

The following is a (very incomplete) list of solution classes:

- Near memory / in-memory computing
- Non-Von Neumann architectures
- Hybrid digital / analog computing
- High density computation: 2.5D, 3D stacking
- Highly integrated compute: cross reticle stitching, multi-chip modules on interposer
- Dataflow and data-aware computing
- ASICs
- Others...

Application specific approaches are acceptable, general approaches which apply to other problem domains are desired
Technical Areas Overview

**TA1 - System Integrator**
- System integration, supporting tools and hardware, as well as a final demonstration

**TA2 - Real-time HPC & Accelerator**
- Design of HPC architecture as well as a hardware accelerator ASICs

**TA3 - General purpose digital RF emulators**
- Design and build emulators which replicate adversary systems

*Not solicited by this BAA*
**Program Metrics (TA1)**

<table>
<thead>
<tr>
<th>Metric</th>
<th>Threshold</th>
<th>Objective</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Number of total systems</strong></td>
<td>80</td>
<td>200</td>
</tr>
<tr>
<td><strong>Minimum latency / range</strong></td>
<td>3.3 µs / 1 km</td>
<td>3.3 µs / 1 km</td>
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<tr>
<td><strong>Maximum latency / range</strong></td>
<td>3300 µs / 2 x 500 km</td>
<td>3300 µs / 2 x 500 km</td>
</tr>
<tr>
<td><strong>Average Tx IBW</strong></td>
<td>1 GHz</td>
<td>1 GHz</td>
</tr>
<tr>
<td><strong>Average Rx IBW</strong></td>
<td>2 GHz</td>
<td>2 GHz</td>
</tr>
<tr>
<td><strong>RCS Complexity</strong></td>
<td>point-cloud model*</td>
<td>high-fidelity model</td>
</tr>
<tr>
<td><strong>Clutter Complexity</strong></td>
<td>discrete clutter</td>
<td>continuous clutter patch</td>
</tr>
<tr>
<td><strong>Multi-path Complexity</strong></td>
<td>10 paths</td>
<td>100 paths</td>
</tr>
<tr>
<td><strong>Environment Update Rate</strong></td>
<td>100 Hz</td>
<td>1 kHz</td>
</tr>
</tbody>
</table>

* 20 discrete scatters or equivalent

The system should be capable of calculating monostatic responses for all connected radars and capable of calculating multi-static responses for a fraction of the connected systems.
Program Metrics (TA2)

<table>
<thead>
<tr>
<th>Metric</th>
<th>TA2 Objective</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum latency</td>
<td>2.5 µs</td>
</tr>
<tr>
<td>Compute (32-bit floating point)</td>
<td>20 PFLOPs</td>
</tr>
<tr>
<td>Total Memory</td>
<td>2.0 Tb</td>
</tr>
<tr>
<td>Aggregate I/O Bandwidth</td>
<td>150 TB/s</td>
</tr>
</tbody>
</table>

Example reference design decomposed into 156 discrete accelerators. Each accelerator required:

- 133 tera floating-point multiply accumulates per second (TMACs)
- 12.2 Gb of memory
- 77 Tb/s of memory bandwidth
- 7.7 Tb/s of input/output (I/O) bandwidth
- Latency less than 2.5 µs.
<table>
<thead>
<tr>
<th>TA1. System Integrator</th>
</tr>
</thead>
<tbody>
<tr>
<td>FY20 Phase 1: DRBE system engineering, design to CoDR</td>
</tr>
<tr>
<td>FY21 Phase 2: DRBE system design to PDR</td>
</tr>
<tr>
<td>FY22 Phase 3: DRBE system design to CDR</td>
</tr>
<tr>
<td>FY23 Phase 4: DRBE system build and integration</td>
</tr>
<tr>
<td>Demo</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TA2. Real-time HPC &amp; Accelerator</th>
</tr>
</thead>
<tbody>
<tr>
<td>FY20 Phase 1: HPC system engineering, design to CoDR</td>
</tr>
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</tr>
<tr>
<td>FY22 Phase 3: Design HPC and firmware to CDR</td>
</tr>
<tr>
<td>FY23 Phase 4: Build HPC and firmware</td>
</tr>
<tr>
<td>Design first-spin ASICs to tapeout</td>
</tr>
<tr>
<td>Fab and test ASICs</td>
</tr>
<tr>
<td>Second-spin design and fab ASICs</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TA3. General purpose digital RF emulators</th>
</tr>
</thead>
<tbody>
<tr>
<td>FY20 Phase 1:</td>
</tr>
<tr>
<td>FY21 Phase 2:</td>
</tr>
<tr>
<td>FY22 Phase 3:</td>
</tr>
<tr>
<td>FY23 Phase 4:</td>
</tr>
<tr>
<td>Design firmware for 3 new RF system emulations</td>
</tr>
<tr>
<td>Build 30 emulators</td>
</tr>
</tbody>
</table>

*Note: “ASIC” simply refers to a chip for the DRBE application and is not meant to express preference for a particular approach*
Proposal content and emphasis
No restrictions proposing to both TA1 and TA2

- You may propose to both TA1 and TA2, but you must submit two separate and independent proposals
  - DARPA may choose to fund neither, one, or both of these proposals
  - If proposing to both:
    - TA1 must not be contingent upon TA2, nor vice-versa
    - TA1 must support other TA2 performers
    - TA2 must support other TA1 performers
Risk tolerance and technical areas (TAs)

- DRBE is a real-time HPC program
- TA2 is the DARPA-hard research-oriented core where high-risk ideas are acceptable
- TA1, and later TA3, are necessary parts of the system where DARPA desires to minimize risk
TA2 guidance
Summary of TA2 Responsibilities

• Design of supporting accelerators which achieves both low latency and high throughput computation

• Integration of the accelerators into a “Real-time HPC” for integration into the larger architecture and tool-suite designed by TA2
• TA2 is anticipated to be entirely unclassified – no need for DoD security infrastructure
• TA2 contracts could be declared fundamental research – eases university participation
  • No grants are offered

• TA2 requires technical expertise in two distinct areas:
  1. Computational accelerators and related technologies (e.g. memory, data transport)
  2. Distributed computing architectures and firmware typical in HPC
  3. RF expertise is nice to have, but TA2 can rely on TA1 for guidance
Accelerator technology

• Computational accelerator technology is the best way to distinguish your proposal from others
  • DARPA prefers to fund a diversity of technologies rather than multiple similar solutions

• “ASIC” is used in the BAA and this presentation as a generic placeholder not intended to guide solutions
  • Proposal of other accelerator technology solutions is encouraged

• What is your proposed semiconductor fabrication process technology?
  • What foundry do you propose to use?
  • Describe IP used. Both external and existing.
  • What are the proposed on-chip technologies for memory, compute, and I/O?
• What is the proposed on-chip architecture?
• What post-fabrication integration technology are you proposing (if any)?

• While high risk is acceptable in TA2, risk is reduced with new designs based on proven technology.
• If your fabrication and post-fabrication integration technologies are not standard, include documentation of their maturity.
HPC architecture

- HPC architecture is the second best way to distinguish your proposal from others.
- Instead of simply proposing an architecture, discuss the architectural tradeoffs you considered and clearly state the advantages of your proposed architecture over alternatives that you rejected.
  - What are the data transport requirements between accelerators?

- Be sure to detail both the number of accelerators expected and the topology/technology which interconnects them

- There is value in a dynamic architecture that supports a diversity of scenarios, or scenarios that vary over time. For example:
  - Number of waveform interactions can increase when RF systems have smaller bandwidth
  - Total number of RF systems can increase so long as some pairs are too far apart to interact

- From the perspective of TA1 and the DRBE system user, what aspects of the HPC capabilities are dynamic? What are the limits of adaptability?
• Include an end-to-end HPC latency budget with line items such as:
  • Interconnect
  • Memory access
  • Signal conditioning filters
  • Environment modeling (e.g., FIR filters)

• Identify anything that is pre-computed to reduce latency. What advance information is required to implement this pre-computation?
• TA2 will work with TA1 to explore design tradeoffs and settle on final requirements.
• Quantify the summary capabilities of your proposed HPC, using the metric in the table below plus other high-level metrics.

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TA1 guidance
Summary of TA1 Responsibilities

• The goal of TA1 is to leverage the RT-HPC designed by TA2 to create the DRBE RF emulation capability.

• Overall Architecture for the DRBE system
  • Interfaces, specifications, and software architecture

• Definition of reference algorithms
  • These define the nature of the calculations that the TA2 system must implement
  • A complete set of algorithms (in chosen high level language) must be provided to TA2 providers

• Radio interface & API

• Supporting software
  • Scenario Design Tools
  • Scenario Controller
  • Resource Management Software
TA1 proposer qualifications

- All TA1 and TA2 hardware is anticipated to be unclassified during development and integration.
- Some test scenario details will be classified at a minimum at collateral Secret
- Some TA3 RF system emulators will be classified at a minimum at collateral Secret
- TA1 proposers require staff and facilities to host preliminary testing at a minimum at the collateral Secret level
- TA1 requires technical expertise in RF systems, RF analysis, propagation, emulation and RF systems experimentation
- Expertise in HPCs and digital hardware is nice to have but is not required.
Threshold and Objective Performance Metrics

• The **threshold** performance metrics are the minimum acceptable capability
• Better performance is desired, with diminishing marginal value beyond the **objective** performance metrics
Trade study with TA2

- Describe the trade study that you propose to conduct with TA2 contractors to refine the allocation of capabilities and requirements between TA1 and TA2.
  - What are the key elements of this trade study and how do they impact both TA1 and TA2?
Scenario performance metrics flowdown

• Qualifications in RF systems analysis and emulation may be illustrated through the ability to flow requirements from the scenario level to the HPC level.
• Starting from the Threshold scenario-level TA1 performance metrics, define a signal flow architecture, required computations, and estimate values for the metrics listed in TA2 preliminary performance metrics.
  • Explain your analysis approach in detail

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As part of this trade study, TA1 will create reference algorithms which demonstrate the desired calculation for core components of the emulation (e.g., the classes of environment response shown earlier)

Your proposal should demonstrate your expertise in RF emulation
Be sure to include what phenomenology you consider key to creating an accurate model of the RF environment
Include your initial (algorithmic) approaches, and why they were chosen
Detail why these approaches will meet the performance metrics given for TA1

The BAA suggests FIR filters to implement waveform interactions. This works for most but not all waveform interactions.
  • Ex: How do you propose to emulate distributed clutter?
  • Do you propose a capability to emulate propagation phenomenology such as atmospheric refraction, knife-edge diffraction, ducting over water, etc? If so, explain the computational approach.
• TA1 is responsible for software tools needed

• Reuse of existing tools is highly desirable over “reinventing the wheel”

• Which of the following TA1 system software components can re-use existing software? Detail the source of the existing software, existing capabilities, and the amount of tailoring required.
  • Scenario design tools
  • Scenario controller
  • HPC resource manager
RF interface

- RF systems normally use an antenna to interface to the environment. Describe how you propose to create the RF interface between such and RF system and the DRBE system.
  - Will the antenna still be used, or will it be circumvented or entirely removed?
  - How will you deal with high-power transmitters?
  - How will you provide coherent signals to multi-channel receivers (e.g. direction-finding array) with each channel having a different phase center?
  - In addition to the RF signal, what other signals must be extracted from, or provided to, the system under test? What sampling/update rate is required for these other signals?

- There is no need for a universal RF interface that can accommodate any RF system. A single interface may be limited to:
  - A range of RF
  - A single type of antenna
  - A class of systems
- What is the total number of unique RF interface variants that you propose to handle your proposed demonstration? (all likely SUTs operating over an RF range from nearly DC to well over 10 GHz)
  - What is the total proposed bandwidth?
• TA1 must develop and test interfaces to the TA2 HPC long before it is available. Describe the TA2 surrogate proposed for use during this time.

• It is acceptable/expected that the surrogate is smaller in scale than the final system.

• When first-run TA2 computational accelerators are available, how can they be tested in the TA2 surrogate?
Design for sanitization

• After running classified test scenarios the entire DRBE system must be sanitized. Propose an approach to design the DRBE system (including HPC) to simplify sanitization and to make Government approval of sanitization procedures more likely.
The program concludes with a demonstration.

What is the nature of your demonstration? How will it highlight the capabilities of DRBE (scale and fidelity)?

What smaller-scale versions of the demonstration will be used to reduce risk throughout the program?

RF SUTs (system under test) will likely be provided by the Government for the final demonstration.

- What GFE / GFI is required?
- Describe SUTs that you propose to use during development and testing prior to the final demonstration.

Describe what must occur before a new SUT is ready for operational testing.

- Will you require SUT modifications or calibration measurements?
- How long will these preparatory steps take?

Identify any type of SUTs that cannot be tested on your proposed DRBE system.
Evaluation Criteria
Evaluation Criteria

1. Overall Scientific and Technical Merit

2. Plans and Capability to Accomplish Technology Transition

3. Cost Realism

4. Potential Contribution and Relevance to the DARPA Mission
The proposed technical approach is innovative, feasible, achievable, and complete.

The proposal quantitatively explains why the proposed approach is expected to meet DARPA’s performance goals specified in Tables 1 and 2. The proposed approach supports all DRBE capabilities as stated in the BAA as well as the implicit or flowed-down requirements.

The proposed technical team has the expertise and experience to accomplish the proposed tasks. Task descriptions and associated technical elements provided are complete and in a logical sequence with all proposed deliverables clearly defined such that a final outcome that achieves the Program goal can be expected as a result of award. The proposal identifies major technical risks, and planned mitigation efforts are clearly defined, feasible, and budgeted.

The proposer’s prior experience in similar efforts clearly demonstrates an ability to deliver products that meet the proposed technical performance within the proposed budget and schedule. The proposed team has the expertise to manage the cost and schedule. Similar efforts completed/ongoing by the proposer in this area are fully described including identification of other Government sponsors.
Technical Area 1 (TA1) – System Integrator

The proposal clearly demonstrates the motivation, plans, and capability to transition DRBE technology and capability to the DoD RF system development, test, and evaluation communities. In addition, the evaluation will take into consideration the extent to which the proposed intellectual property (IP) rights structure will potentially impact the Government’s ability to transition the technology.

Technical Area 2 (TA2) – Real-time HPC and Hardware Accelerator

The proposal identifies additional applications for high-throughput real-time HPC technology, which may include both DoD and commercial applications. The proposal clearly demonstrates the motivation, plans, and capability to transition DRBE technology to both the primary DRBE application as well as the other applications identified by the proposer. In addition, the evaluation will take into consideration the extent to which the proposed intellectual property (IP) rights structure will potentially impact the Government’s ability to transition the technology.
The proposed costs are realistic for the technical and management approach and accurately reflect the technical goals and objectives of the solicitation. The proposed costs are consistent with the proposer's Statement of Work and reflect a sufficient understanding of the costs and level of effort needed to successfully accomplish the proposed technical approach. The costs for the prime proposer and proposed subawardees are substantiated by the details provided in the proposal (e.g., the type and number of labor hours proposed per task, the types and quantities of materials, equipment and fabrication costs, travel and any other applicable costs and the basis for the estimates).

Note that the evaluation criteria is “Cost Realism” not “Cost”. Undue emphasis on cost may motivate proposers to unjustifiably lower the proposed cost and thus lower the evaluation score for Cost Realism. Attempts to lower cost through planning to use too many junior personnel may negatively impact the evaluation score for Overall Scientific and Technical Merit.

For efforts with a likelihood of commercial application, appropriate direct cost sharing may be a positive factor in the evaluation of Cost Realism.
The potential contributions of the proposed effort are relevant to the national technology base. Specifically, DARPA’s mission is to make pivotal early technology investments that create or prevent strategic surprise for U.S. National Security.

The proposer clearly demonstrates its plans and capabilities to contribute to U.S. national security and U.S. technological capabilities. The evaluation will consider the proposer’s plans and capabilities to transition proposed technologies to U.S. national security applications and to U.S. industry. The evaluation may consider the proposer’s history of transitioning or plans to transition technologies to foreign governments or to companies that are foreign owned, controlled, or influenced. The evaluation will also consider the proposer’s plans and capabilities to assist its employees and agents to be eligible to participate in the U.S. national security environment.
Proposers Day Summary
Proposers Day Summary

Only TA1 & TA2 submissions being accepted

Proposal Due Date: April 1, 2019
Estimated period of performance start: September 2, 2019

No live Q&A today
All FAQ topics will received through email and posted to FBO
FAQ submission cut off: March 18, 2019
FAQ submission email: HR001119S0023@darpa.mil

Don’t forget: 1) Task Staffing Summary, and 2) Proposal Summary Chart