Photonics in the Package for Extreme Scalability (PIPED)

Gordon Keeler, PM, DARPA/MTO

Proposers Day
November 1, 2018
The Data Movement Challenge

**Motivation:** Achieve system performance gains by scaling up and out...

**in-package**
NVIDIA Tesla V100
GPU accelerator
5120 cores
125 teraflops, 300 W, $5K

**board level**
NVIDIA DGX-2
Enterprise AI
16 GPUs
2 petaflops, 10 kW, $400K

**multi-rack**
IBM Summit
Top supercomputer
36,864 GPUs & CPUs
200 petaflops, 13 MW, $300M

**Problem:** Package I/O is limited in bandwidth, power, latency, reach...

- **I/O power exceeds full socket allocation**
- **bandwidth per socket**
- **total power per package**
- **power for off-chip I/O**

Images courtesy of NVIDIA and IBM
**PI PES Targets**

**Objective:** Enable disruptive system scalability through embedded photonic I/O to increase package bandwidth by 100x, reduce I/O power 100x, and extend reach 10,000x.

**Distribution Statement A:** Approved for public release. Distribution is unlimited.
### State-of-the-art Electronic Signaling

#### Wide variety of engineering solutions

<table>
<thead>
<tr>
<th>on chip</th>
<th>in package</th>
<th>on board</th>
</tr>
</thead>
<tbody>
<tr>
<td>wiring on monolithic die</td>
<td>wiring on MCM/SiP</td>
<td>PCB, cables, pins, connectors</td>
</tr>
<tr>
<td>• simple gate-to-gate link</td>
<td>• AIB, UIB, USR, HBM</td>
<td>• PCI-E, LVDS, DDR, SERDES...</td>
</tr>
<tr>
<td>• full-swing, voltage mode</td>
<td>• serial/fast or parallel/wide</td>
<td>• current-mode serial links</td>
</tr>
<tr>
<td>• &lt;100μm or repeaters</td>
<td>• moderate complexity</td>
<td>• high complexity</td>
</tr>
<tr>
<td>• 1-100 fJ/bit</td>
<td>• 0.1-2 pJ/bit</td>
<td>• 2-20 pJ/bit</td>
</tr>
</tbody>
</table>

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**Diagram:**
- **core IC**
- **SERDES**
- **interposer**
- **package**
- **PCB**
State-of-the-art Electronic Signaling

Wide variety of engineering solutions

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</table>

But physics sets clear trends

High nonlinear roll-off due to:
- channel bandwidth limits,
- circuit bandwidth limits,
- circuit overhead/complexity

work here!
Interconnect Figure of Merit

BW Density * Energy Efficiency (Gbps/mm)/(pJ/bit)

Max Interconnect Distance (meters)

NVIDIA GRS 2013, ISSCC 2018

Mixed Signal: LVDS
32nm SerDes
65nm SerDes
HBM

3D: CHIPS LR
CHIPS SR

Optical: Finisar BOA/MBOM
Finisar 100 GBASE SR4 QSFP28
Mellanox 100 GbE CPRI QSFP28
Mellanox 100 GbE SR4 QSFP28
Avago Micropod

In-package
On-board
Off-board

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Interconnect Figure of Merit

![Graph showing the relationship between density, energy efficiency, and interconnect distance.](Images from Mellanox and Samtec)
Interconnect Figure of Merit

PIPES seeks to remove data locality as a design bottleneck, extending socket-level I/O performance system-wide.

**TA1:** 100 Tbps, 1 pJ/bit

**TA2:** 1 Pbps, 100 fJ/bit

PIPES goals

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.
Facilitating DoD Access: Create an ecosystem for package-level optical signaling, enabling disruptive advances for artificial intelligence, phased arrays, sensors and processing.
Technology Transition with DoD Relevance

**Capability providers**
- photonic component fab
- optical chiplets, IP blocks
- interface definition
- optical and electrical packaging with custom ASICs

**Commercial Participants**
- build partnership business model and supply chain
- develop collaborations and discuss joint standards

**DoD Users**
- leverage packaged MCMs
- access technologies for custom designs with new ASICs
- license IP, access trusted suppliers, on-shore packaging
- help define requirements, build prototypes, drive early adoption

**Exercising the Ecosystem**
- teaming and collaboration through PIPES discussions and “demo phase” activities

**DARPA investment**
- fill technology gaps,
- connect stakeholders

Performers across all TAs have a role in the PIPES Ecosystem
Technical Areas
Desired Outcomes of PIPES

Technical Goals and Expectations:

• Develop high-value MCMs (ASIC, FPGA, GPU, CPU, ...) with in-package photonic I/O yielding energy, density, and bandwidth >10x beyond today. (TA1)

• Create & exercise a path to transition PIPES technologies to DoD users. (TA1B)

• Develop scalable, manufacturable technologies with performance well beyond current SOTA for 2025-era photonic I/O. (TA2 and TA3)

• Enable domestic capabilities for high-density, low-loss photonic and electronic packaging. (TA1 and TA3)

• Maintain familiar form factors consistent with current practice for advanced ICs, including dimensions, electrical interfaces, and thermal management. (All TAs)

DoD Technology Transition:

• Enable sustained access for the U.S. Government and its contractors to the technologies and capabilities developed under PIPES. (All TAs)
TA1: Photonically-Enabled Multi-Chip Modules (MCMs)

Objective
- Enable **disruptive microelectronics** by embedding photonics in FPGA, GPU, ASIC
- Drive link **energy, density, and BW 10x** beyond current R&D results
- Establish **DoD-accessible ecosystem** for photonically-enabled 2.5D microelectronics

Key Metrics and Deliverables
- Create **enduring domestic capability** for manufacturing and packaging
- **100 Tbps I/O** per IC package (10x SOTA)
- **1 pJ/bit** efficiency (10x SOTA)
- 20 meter reach / 100 ns latency
- Packaged **mission-relevant MCM demo**

Key Challenges
- high-volume manufacturing & low parasitics
- low-loss fiber coupling & multiplexing
- compact, low-energy Tx/Rx circuits
- high-order multiplexing

Leverage and extend recent R&D innovation for DoD system insertion
Technical Area 1
Photonically-Enabled MCMs (6.3)

- **Anticipated Funding**
  - 6.3 funding
  - $35M / 42 months
  - Multiple awards

- **Major Deliverables**
  - Phase 2 - Two packaged 10T, 1 pJ/bit demonstrator units; Ten packaged, fully operational MCMs
  - Phase 3 - Two packaged 100T, 1 pJ/bit demonstrator units; Detailed transition plan to implement technology in PIPES ecosystem

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Phase 1: Components
- CDR: 6 mo.
- Packaged prototype: 2.5 pJ/bit
  10 Tbps/pkg

Phase 2: Integration
- MCM system
  - 10T demo: 1.0 pJ/bit fully-packaged

Phase 3: Scalability
- 100T demo: DoD accessible modular capability with packaging
# TA1: Photonically Enabled MCMs

<table>
<thead>
<tr>
<th></th>
<th>Phase 1</th>
<th>Phase 2</th>
<th>Phase 3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Key outcomes</strong></td>
<td>10T technology demonstration*</td>
<td>Enhanced 10T demo* AND Packaged MCM demo</td>
<td>100T technology demo* AND Differentiating Access</td>
</tr>
<tr>
<td>Aggregate bandwidth</td>
<td>10 Tbps</td>
<td>10T demo: 10 Tbps MCM: proposer defined</td>
<td>100 Tbps</td>
</tr>
<tr>
<td>Energy per bit</td>
<td>2.5 pJ/bit</td>
<td>1 pJ/bit</td>
<td>1 pJ/bit</td>
</tr>
<tr>
<td>Edge bandwidth density</td>
<td>1 Tbps/mm</td>
<td>2 Tbps/mm</td>
<td>2 Tbps/mm</td>
</tr>
<tr>
<td>Link latency</td>
<td>200 ns + TOF</td>
<td>100 ns + TOF</td>
<td>100 ns + TOF</td>
</tr>
<tr>
<td>Link reach (between packages)</td>
<td>20 meters</td>
<td>20 meters</td>
<td>20 meters</td>
</tr>
<tr>
<td>Bit error ratio (BER)</td>
<td>$10^{-9}$</td>
<td>$10^{-12}$</td>
<td>$10^{-12}$</td>
</tr>
<tr>
<td>Link margin</td>
<td>0 dB</td>
<td>2 dB</td>
<td>4 dB</td>
</tr>
<tr>
<td>Packaged units delivered</td>
<td>--</td>
<td>2x 10T demo units</td>
<td>2x 100T demo units</td>
</tr>
<tr>
<td>Operating temperature range</td>
<td>--</td>
<td>Room temperature to 80°C</td>
<td>Room temperature to 80°C</td>
</tr>
<tr>
<td>Solder reflow compatible</td>
<td>--</td>
<td>250°C, 5 min</td>
<td>250°C, 5 min</td>
</tr>
<tr>
<td>Integration and optical packaging technique</td>
<td>manual assembly</td>
<td>manual assembly</td>
<td>automated</td>
</tr>
<tr>
<td>Total port count</td>
<td>proposer defined</td>
<td>proposer defined</td>
<td>proposer defined</td>
</tr>
</tbody>
</table>

* Technology demonstrators are satisfied by co-packaging optical I/O with a proxy IC core to generate and receive data streams.
Proposal Elements:

1. Describe the application and interconnect requirement. How is the problem addressed today and what are the limitations of the current approach?

2. Clearly show the expected benefit to the DoD mission by projecting the differential advantage provided to the Warfighter.

3. Outline the technical requirements for the photonically-enabled MCMs and optical I/O capabilities accessed through the PIPES ecosystem.

4. Collaboration with a TA1 proposer at the proposal stage is encouraged but not required. It is expected that a TA1 partner will be identified and an Associate Contractor Agreement (ACA) will be signed no later than the end of Phase 1.
TA1B: Defense Applications and Demonstration

Apply TA1 technology to a high-value mission of interest to the DoD.

Technical Area 1

Phase 1: Components

Phase 2: Integration

Phase 3: Scalability

Technical Area 1B
DoD Applications
(6.3)

ACA = Associate Contractor Agreement

- Anticipated Funding
  - 6.3 funding
  - 24 months
  - NTE $600K per award
  - Multiple awards

- One or more performers may be selected for a final 18-month demonstration phase.
- DARPA reserves the right to solicit and select proposals from performers other than those initially selected in TA1B.

DoD Application Demo
- For reference only -
- Not to be proposed -
TA2: Photonics for Massive Parallelism

**Objective**
- Develop emerging photonics components and architectures for performance **100x beyond SOTA** to enable future scaling
- Establish feasibility and path to domestic manufacturing

**Key Metrics and Deliverables**
- Demonstrate prototype link performance
- **I/O scalable to 1 Pbps (100x SOTA)**
- **0.1 pJ/bit efficiency (100x SOTA)**
- 100 meter reach / <50 ns latency
- Demonstrate scalability to 100 Tbps

**Enabling a Capability for 1 Pbps**

**Key Challenges**
- power reduction
- electronic integration
- component density
- materials integration
- packaging complexity

Enable distributed parallelism through next-generation photonic links
Technical Area 2
Photonics for Massive Parallelism (6.2)

Component-based link demo
perf. consistent w/ integrated system

Integrated link
0.2 pJ/bit
one 10 Tbps port

1P technology
0.1 pJ/bit
ten 10 Tbps ports, scalable to 1 Pbps

• Anticipated Funding
  o 6.2 funding
  o $20M / 42 months
  o Multiple awards

• Major Deliverables
  o Phase 2 - Two packaged 10T, 0.2 pJ/bit demonstrator units;
  o Phase 3 - Two packaged 100T, 0.1 pJ/bit demonstrator units;
    Detailed transition plan to implement technology in PIPES ecosystem
<table>
<thead>
<tr>
<th>Key outcomes</th>
<th>Phase 1</th>
<th>Phase 2</th>
<th>Phase 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Benchmark component demonstration performance traceable to link prototype</td>
<td>Integrated link demonstration performance traceable to scaled system</td>
<td>Scaled multi-port I/O demonstration performance consistent with 1 Pbps capability</td>
<td></td>
</tr>
<tr>
<td>Energy per bit</td>
<td>0.5 pJ/bit</td>
<td>0.2 pJ/bit</td>
<td>0.1 pJ/bit</td>
</tr>
<tr>
<td>Areal bandwidth density</td>
<td>5 Tbps/mm²</td>
<td>5 Tbps/mm²</td>
<td>5 Tbps/mm²</td>
</tr>
<tr>
<td>Aggregate bandwidth</td>
<td>proposer defined</td>
<td>10 Tbps</td>
<td>100 Tbps</td>
</tr>
<tr>
<td>Total port count</td>
<td>--</td>
<td>≥ 1</td>
<td>≥ 10</td>
</tr>
<tr>
<td>Link latency</td>
<td>--</td>
<td>100 ns + TOF</td>
<td>50 ns + TOF</td>
</tr>
<tr>
<td>Link reach (between packages)</td>
<td>1 meters</td>
<td>10 meters</td>
<td>100 meters</td>
</tr>
<tr>
<td>Bit error ratio (BER)</td>
<td>$10^{-9}$</td>
<td>$10^{-12}$</td>
<td>$10^{-12}$</td>
</tr>
<tr>
<td>Hardware delivered</td>
<td>--</td>
<td>2 demo units</td>
<td>2 demo units</td>
</tr>
<tr>
<td>Operating temperature range</td>
<td>--</td>
<td>Room temperature to 80°C</td>
<td>Room temperature to 80°C</td>
</tr>
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DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.
TA3: Interconnect Fabrics

Objective

- Develop **key technologies essential** to mature and amplify the impact of TA1/TA2
- Two areas identified to enable next-generation distributed parallelism:
  - optical packaging
  - reconfigurable switching

Approach and Goals

- Smaller investments to study thrust areas independent from TA1/TA2 link efforts
- **Packaging:** create scalable approaches for low-loss optical packaging and high-port count fiber connectivity
- **Switching:** develop efficient reconfigurable optical switch fabrics

Path to Flexible & Scalable Architectures

Key Challenges

- massive port count
- static routing complexity
- dynamic reconfigurability

Develop deployable technologies for distributed computing architectures

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TA3: Interconnect Fabrics

TA3 seeks high-risk, high-payoff approaches to enable future scaling beyond what will be developed elsewhere within the program.

Technical Area 3
Interconnect Fabrics (6.2)

- **Concept**
  - 18 months
  - approaches validated components demonstrated

- **Integrated capability**
  - 12 months

- **Demonstrated scalability**
  - 12 months

**Anticipated Funding**
- 6.2 funding
- $10M / 42 months
- Multiple awards in two thrust areas

**Major Deliverables**
- Phase 2 - Report documenting performance of integrated devices; Commercialization strategy white paper;
- Phase 3 - Two packaged demonstrator units (switching thrust); Detailed transition plan to implement technology in PIPES ecosystem (packaging thrust)
### TA3: Interconnect Fabrics

<table>
<thead>
<tr>
<th>Thrust</th>
<th>Phase 1</th>
<th>Phase 2</th>
<th>Phase 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-density optical packaging and routing</td>
<td>Concept demonstration*</td>
<td>Integration demonstration**</td>
<td>Volume-compatible optical packaging capability</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1,000+ fibers out of the package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Target insertion loss &lt; 0.25 dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Insertion loss not to exceed 1 dB over 100 nm spectral bandwidth</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Automated alignment/attach</td>
</tr>
<tr>
<td>Reconfigurable optical switching technologies</td>
<td>Concept demonstration*</td>
<td>Integration demonstration**</td>
<td>Integrated switch meeting performance targets</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1,000 x 1,000 or greater switch matrix</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Fiber-to-fiber insertion loss below 3 dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Switch reconfiguration time below 10 μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Spectral bandwidth &gt; 100 nm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Switch power &lt; 100 W</td>
</tr>
</tbody>
</table>

* Phase 1 metrics are user-defined and must establish the feasibility of the technical approach, highlighting the ability of the concept to meet the ultimate metrics of the thrust.

** Phase 2 metrics are user-defined and must establish confidence in the technical approach, while demonstrating that the technology is capable of scaling to high port counts with low optical losses, and consistent with the ultimate metrics of the thrust.
A Note on Link Budget: Power/Energy Estimates

### Optical Link Budget
- Lasers
- Couplers
- Modulators
- Passives
- Channel
- Photodiodes

### Electronics Power Consumption
- Interconnect from/to transistor layer
- Serialization / Deserialization
- Thermal tuning
- Modulator / Demodulator
- Receiver: detector, amplifier, …
- Misc: clock, DSP, CDR, EC, EQ…

Include Everything in Energy/Bit Estimates
Important Dates

• BAA Posting Date: October 31, 2018
• Proposers Day: November 1, 2018
• Abstract Due Date: **November 20, 2018 at 1:00 PM**
• FAQ Submission Deadline: January 3, 2018 at 1:00 PM
• Proposal Due Date: **January 17, 2019 at 1:00 PM**
  - Rolling deadline: DARPA will continue to accept full proposals until March 1, 2019 at 1:00 PM.
  - If deemed compliant, such proposals will be reviewed at the Government’s discretion, contingent upon the availability of funds.
  - Proposers are warned that the likelihood of available funding is greatly reduced for proposals submitted after the initial closing date deadline.
• Estimated period of performance start: July 2019

Questions: [HR001119S0004@darpa.mil](mailto:HR001119S0004@darpa.mil)
Evaluation Criteria, in Order of Importance

1. Overall Scientific and Technical Merit
   - Demonstrate that the proposed technical approach is innovative, feasible, achievable, and complete.
   - Describe how the proposed approach will achieve each program metric with sufficient detail and supporting experimental measurements, modeling, calculations, and/or simulations.

2. Potential Contribution and Relevance to the DARPA Mission
   - Note the updated wording, with an emphasis on contribution to U.S. national security and U.S. technological capabilities.
   - Discuss how the proposed effort addresses the ERI goals of technology transition and facilitating access to PIPES technologies for the DoD.

3. Cost Realism
   - Ensure proposed costs are realistic for the technical and management approach and accurately reflect the goals and objectives of the solicitation.
   - Verify that proposed costs are sufficiently detailed, complete, and consistent with the Statement of Work.
# Proposers Day Agenda

<table>
<thead>
<tr>
<th>Time</th>
<th>Activity</th>
<th>Speaker</th>
</tr>
</thead>
<tbody>
<tr>
<td>0800-0830</td>
<td>CHECK-IN</td>
<td></td>
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<tr>
<td>0830-0900</td>
<td>Poster Setup and Breakfast</td>
<td></td>
</tr>
<tr>
<td>0900-0915</td>
<td>Welcome - Security, Logistics</td>
<td>Mr. Ron Baxter</td>
</tr>
<tr>
<td>0915-0930</td>
<td>Introduction to MTO and the ERI</td>
<td>Dr. William &quot;Bill&quot; Chappell</td>
</tr>
<tr>
<td>0930-1030</td>
<td>Program Overview</td>
<td>Dr. Gordon Keeler</td>
</tr>
<tr>
<td>1030-1100</td>
<td>Contracting Overview</td>
<td>Mr. Michael Blackstone</td>
</tr>
<tr>
<td>1100-1130</td>
<td>Lightning Round</td>
<td>Proposers</td>
</tr>
<tr>
<td>1130-1230</td>
<td>LUNCH (Provided)</td>
<td></td>
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<tr>
<td>1230-1300</td>
<td>Question and Answer Session</td>
<td>Dr. Gordon Keeler</td>
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<tr>
<td>1300-1500</td>
<td>Posters</td>
<td></td>
</tr>
<tr>
<td>1330-1700</td>
<td>One-On-One Meetings with PM</td>
<td>(by request/appointment)</td>
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