CRAFT:
Circuit Realization At Faster Timescales

Linton G. Salmon

Proposers Day

August 20, 2015

Today's Agenda

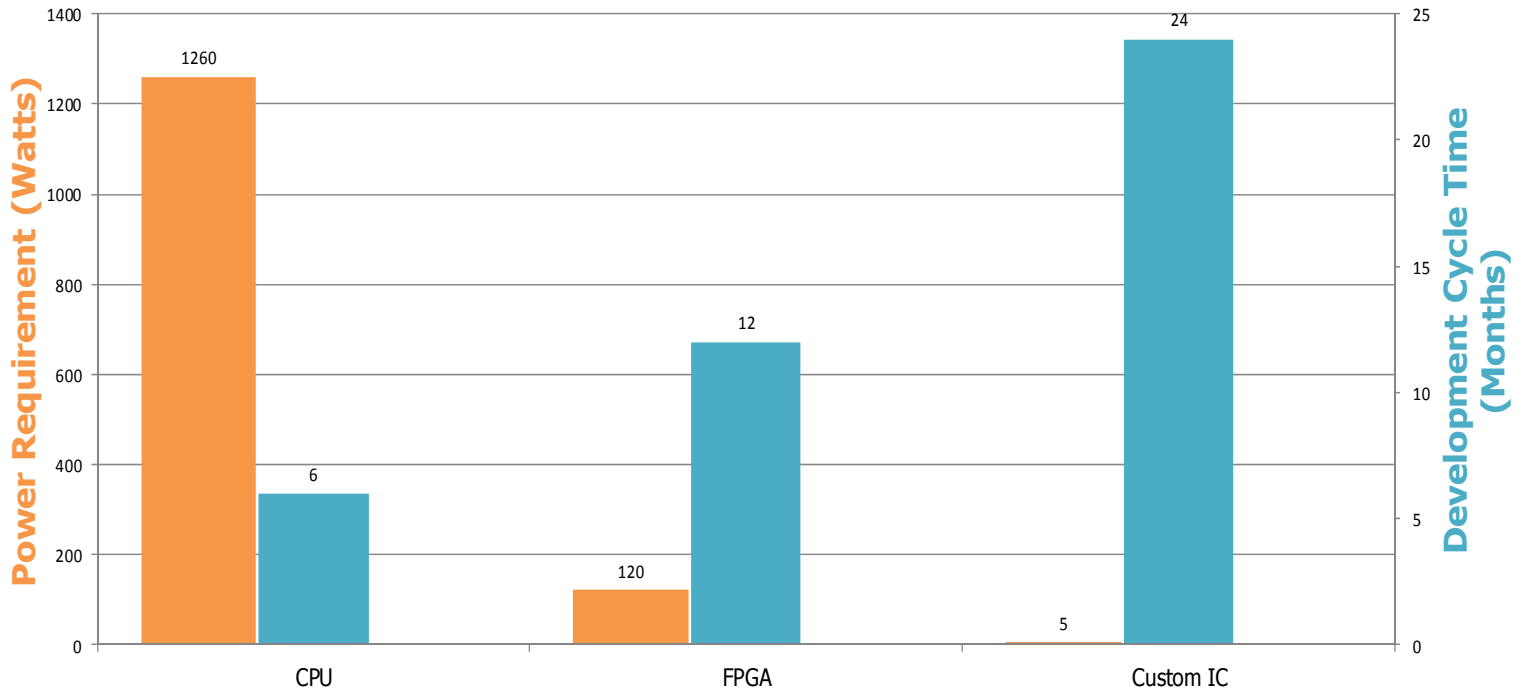
Agenda

Time		Event	Speaker
7:00AM	8:00AM	*Registration Check-in*	*(Hahn Auditorium Lobby)*
8:00AM	**8:10AM**	**Welcome / Ground Rules**	Linton Salmon
8:10AM	**10:00AM**	**CRAFT Overview**	
10:00AM	10:15AM	*Morning Break*	-
10:15AM	**10:35AM**	**Q&A Session**	Linton Salmon
10:35AM	10:40AM	*Break*	-
10:40AM	**11:30AM**	**Guest Presentations:**	
10:40AM	10:45AM	Google, Inc.	Amir Salek
10:45AM	11:00AM	ARM	Eric Hennenhoefer
11:00AM	11:30AM	Ambiq Micro	Mike Noonen
11:30AM	12:30PM	*Lunch Break / Private Poster Session*	-
12:30PM	1:00PM	*Break*	-
1:00PM	**5:00PM**	**Open Poster Session / Teaming**	*(Hahn Auditorium Lobby)*
1:00PM	**5:00PM**	**One-on-One Breakout Sessions**	*(Green Room)*
5:30PM		*Adjourn*	

Motivation for CRAFT

Performance versus Development Cycle Times

Today you have to choose between performance and schedule/cost.



Example Data from representative DoD design

	Qty	Power Req.	Dev. Cycle Time	Current Character
General Purpose Central Processor **(CPU)**	28	**1260W**	**~6 months**	Low performance at power Flexible Quick to implement
Field Programmable Gate Array **(FPGA)**	4	**120W**	**~12 months**	Low performance at power Flexible Moderately quick to implement
Custom Integrated Circuit **(Custom IC)**	1	**5W**	**~24 months**	High performance at power Relatively inflexible Slow to implement

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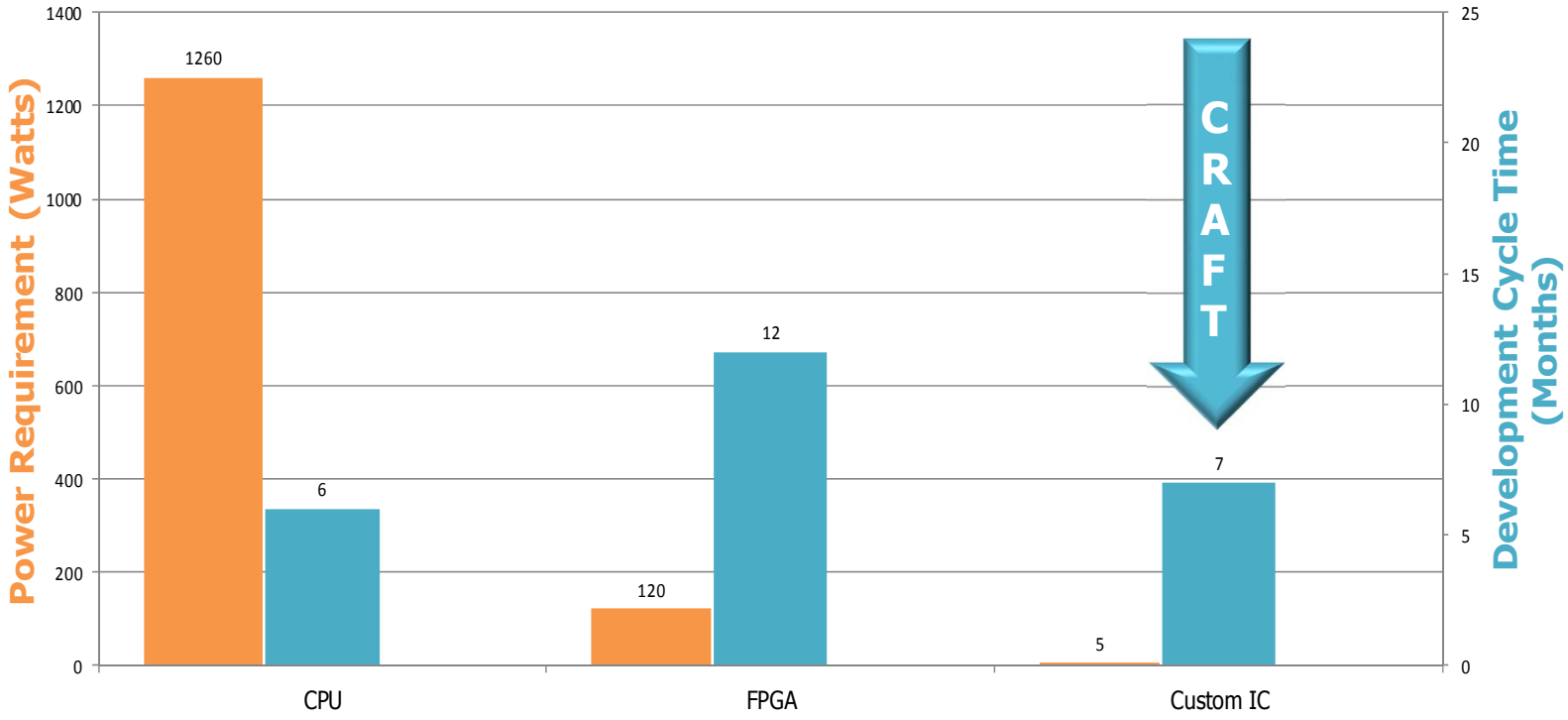
Performance versus Development Cycle Times

CRAFT Vision

To sharply reduce the barriers to DoD use of custom integrated circuits built using leading-edge CMOS technology while maintaining the high level of performance at power promised by this technology.



Commercial and DoD Access to Leading-Edge CMOS Technology

Current Status

Commercial

- Most volume at 28nm
- Leading-edge products shipped at 20nm
- Pilot production at 16nm/14nm
  - Driven by large companies
  - PDK widely available 2Q14
- All leading-edge processes bulk
- Leading-edge technology available at multiple facilities
- Turnaround time: 2-4 months (28nm)

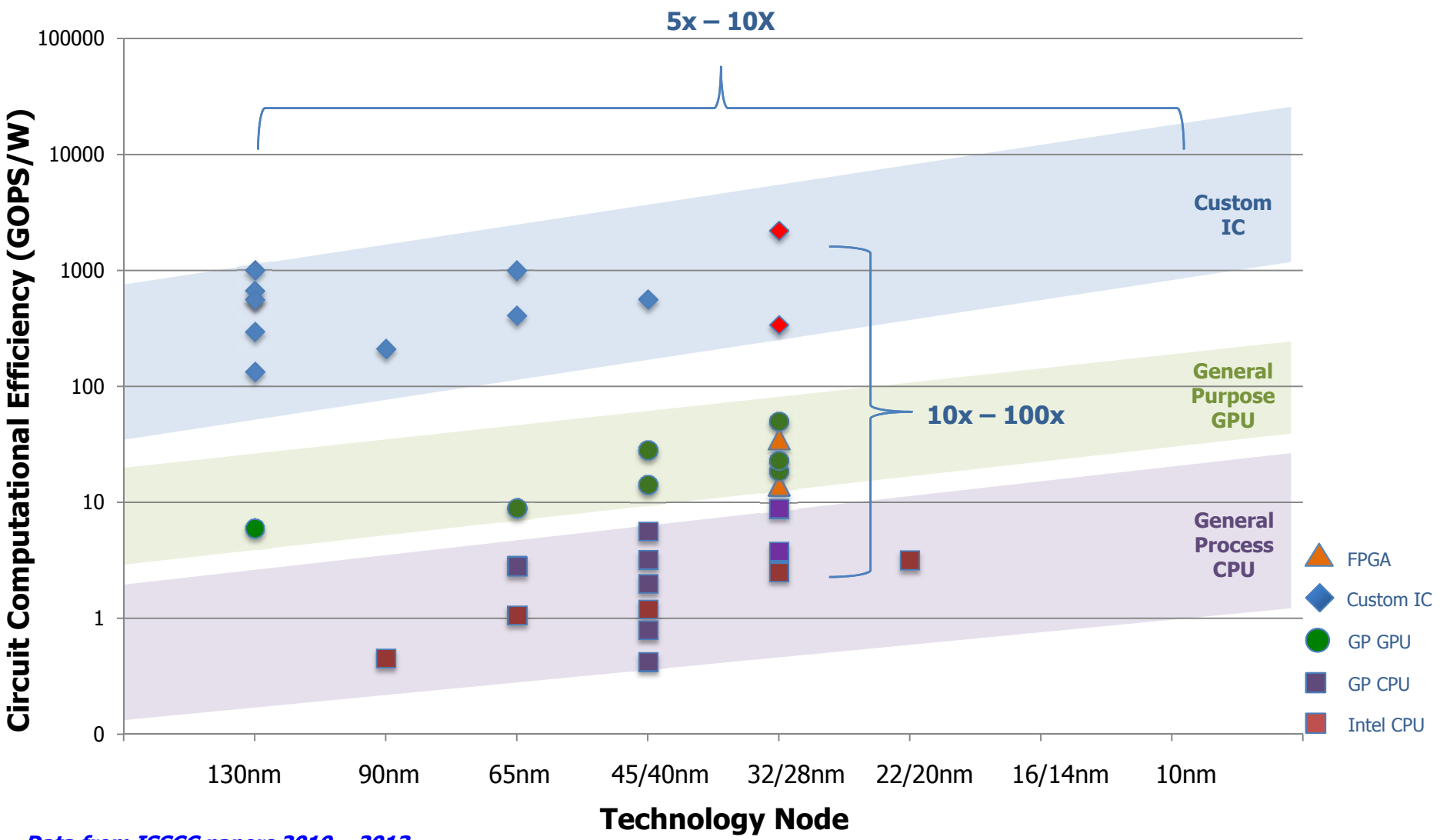
DoD

- Most volume at ≥ 130nm
- Leading-edge products shipped at 90nm
- Pilot production at 45nm
  - Driven by availability of infrastructure
  - ~ 3 nodes behind 16nm/14nm
- All leading-edge processes SOI
- Leading-edge technology confined to one at-risk facility, IBM–East Fishkill
- Turnaround time: 9-12 months (32nm)

Need

- √ Greatly improved design methodology to sharply reduce design time/effort
- √ Regular, dependable, fast leading-edge CMOS multiple-project runs for DoD
- √ Full, supported commercial design enablement from foundry
- √ A common methodology for DoD-specific IP generation/distribution
- √ Facilitated commercial component circuit (IP) access

Why Use Leading-Edge CMOS Custom Integrated Circuits?



Data from ISSCC papers 2010 – 2013
and "Energy Efficient Computing on Embedded and Mobile Devices" on nVidia.com

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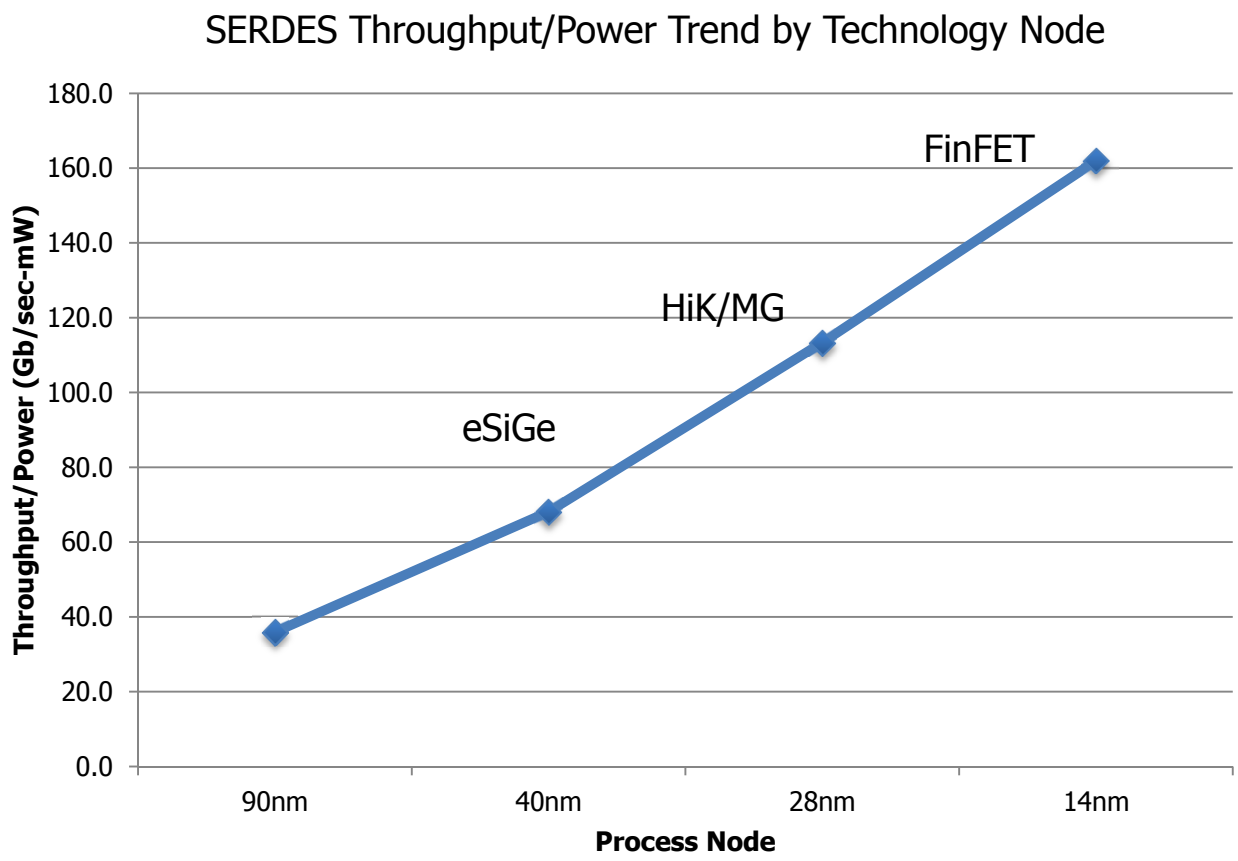
Improvement with Technology Node Continues



- High-speed circuit performance continues to improve with process node
- Improvements driven by new process technology/materials and increased number of transistors available, not just lithography

Now is the Time to Design Using 16nm/14nm Technology

Epiphany IV
- Simple, general purpose GPU chip, not a full SoC
- Application chosen to meet resource availability
- Modularity of design driven by application
- However, example of possibilities with CRAFT

CRAFT-enabled custom IC for DoD
- Full, targeted custom IC implementation
- Application chosen to meet a DoD need
- Modularity of design driven by CRAFT
- Similar schedule/level of effort as Epiphany IV

5-person design team
12 weeks to design
28nm fabrication
50 GOPS/W
Designed in 2011
Around PDKV1.0 release

Image from A Oloffson of Adapteva

10-person design team
16 weeks to design
16nm/14nm fabrication
> 1000 GOPS/W
To be designed in 2016
Around PDK V2.0 release

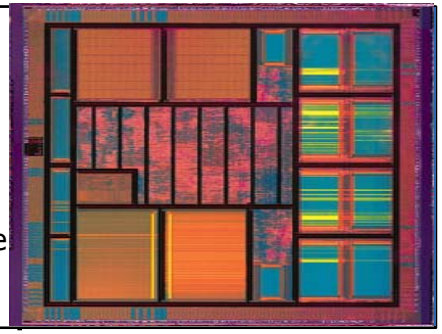
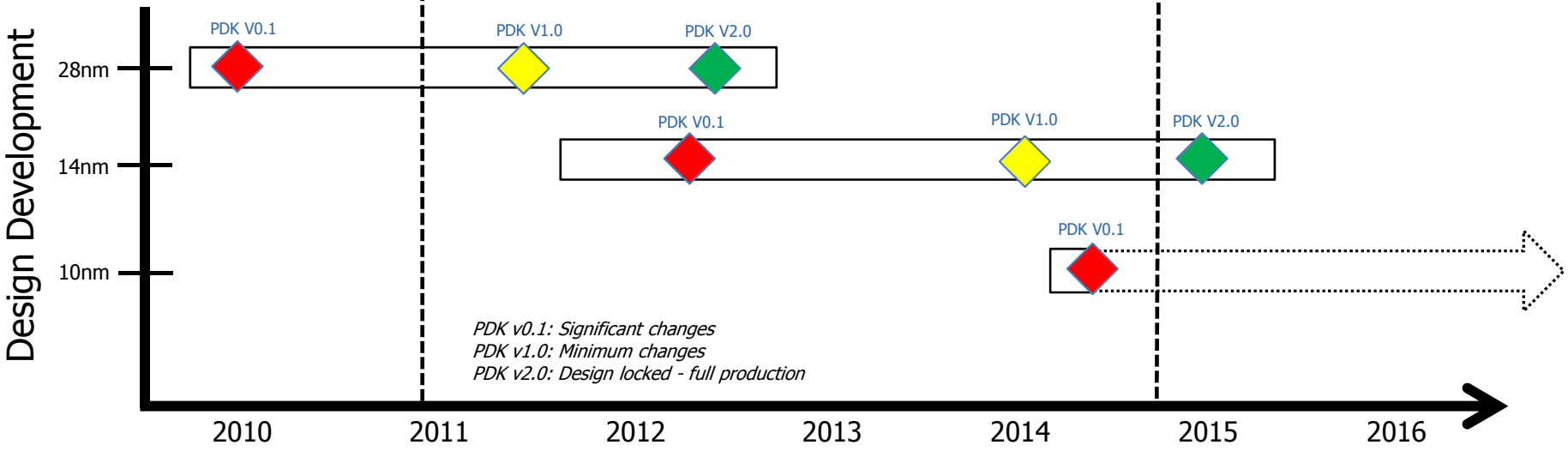


Image from Wikimedia Commons



Proposed Shuttle Details

- Proposed 16nm/14nm FinFET process flow
  - Bulk FinFET transistors with dual gate oxide
    - SVT/LVT/1.8V IO transistor
  - BEOL stack: 9 levels of Cu wiring
    - 1-M1/2-Mx/2-1.3x/2-2x/2-11x
  - Standard passive components (no deep trench capacitor)
  - Standard eFuse and anti-fuse blocks
  - HP SRAM bit cell
- Tentative schedule
  - PDK available: September, 2015
  - Training: October - December, 2015
  - Firm shuttle commitment from users required: November, 2015
  - Design submission (GDS-In): February, 2016
  - Die back to users: August, 2016 (GDS-In + 6 months)
- Aggregator/interface/training organization
  - All questions for the foundry will go through foundry interface
  - All GDS will be sent to aggregator
- User cost will be ~ $50K/(3mmX2mm) project

Current Design Flow Takes So Long that it is Throttling DoD Access to Advanced Technology

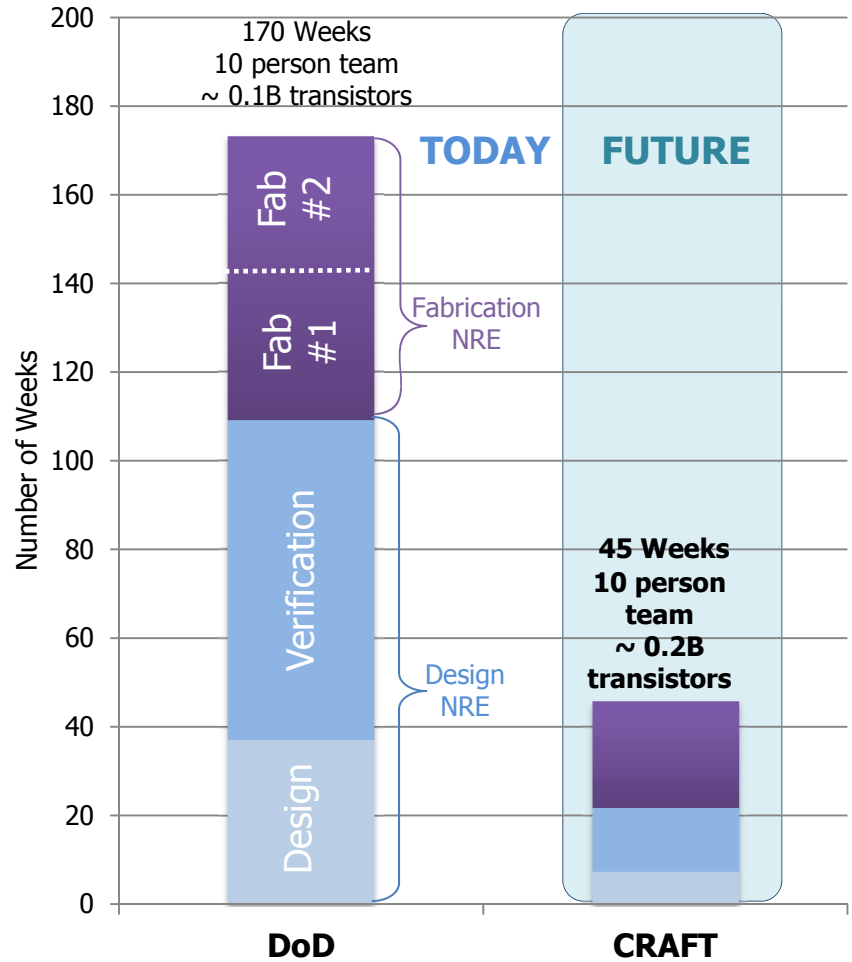
Existing DoD custom IC product cycle time can take as long as **2.5 years**.

- 60%: Design (most of which is verification)
- 40%: Fabrication (20%/fab spin)

Using "Object Oriented Design" and enhanced hierarchy, we want to achieve:

- Reduction in design time by 10X through a strong reduction in verification time and removal of minimum area constraint
- "First Time Right" design methods to eliminate the need for repeated fabrication runs.
- Reduction in fabrication time to 2X commercial

14nm node example



Data from industry survey by DARPA consultants

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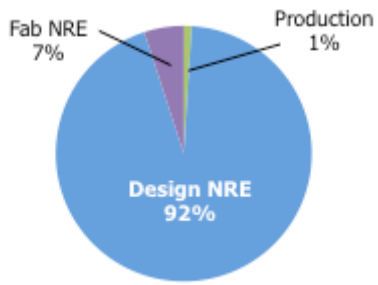
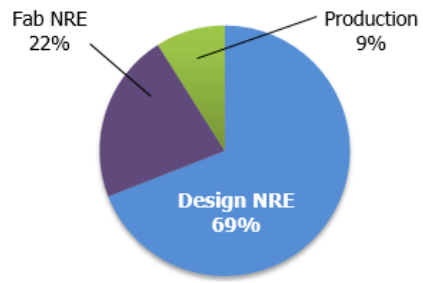
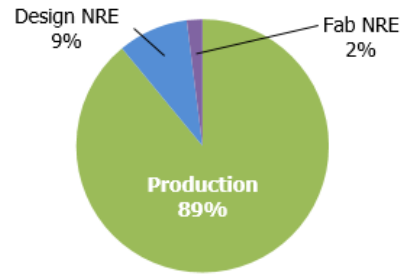
Market Differences

	Low Volume	Moderate Volume Commercial	High Volume Commercial
			
Design Cost	Major contributor to total SoC cost	Major contributor to total SoC cost	Minor portion of total SoC cost
Fabrication Cost	Small contributor to total SoC cost	Significant contributor to total SoC cost	Major contributor to SoC cost
Volume	1k parts	1,000k parts	100,000k parts
Area	Not important	Relatively unimportant	Critical
Design Schedule/Risk	Critical	Critical	Critical
Performance at Power	Required	Required	Required

High-Level Description of CRAFT

CRAFT: Enabling Use of the Best Commercial Technology

CRAFT aims to provide solutions to the three major obstacles restricting custom IC design and fabrication for DoD systems.

DESIGN

- Design requires 18-24 months of effort
- Design verification takes far too much effort
- Fab cycles are too long and too uncertain
- Access to leading-edge CMOS is difficult

CRAFT aims to create new design flows that will reduce custom IC design cycle time by ***10x*** and increase design robustness through object-oriented design techniques

PORT/ MIGRATE

- Designers are limited to one foundry
- Migration of designs from one node to another is difficult and expensive

CRAFT aims to use new design flows to ensure multiple sources of supply and reduce node migration effort by 80% to keep DoD out of "the Silicon Ghetto"

REPOSITORY

- Severe lack of IP reusability for DoD designs
- Current audit model for custom IC design/hardware security is broken

CRAFT aims to establish a data location and methodology to ensure 50% IP* reuse by DoD performers

CRAFT 's goal is to enable more efficient custom IC design/fabrication to enable HIGH performance electronic solutions FASTER and with more FLEXIBILITY

* IP – Sub-circuits used for modern custom ICs

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We Need a New Custom IC Design Flow

New Software Tool

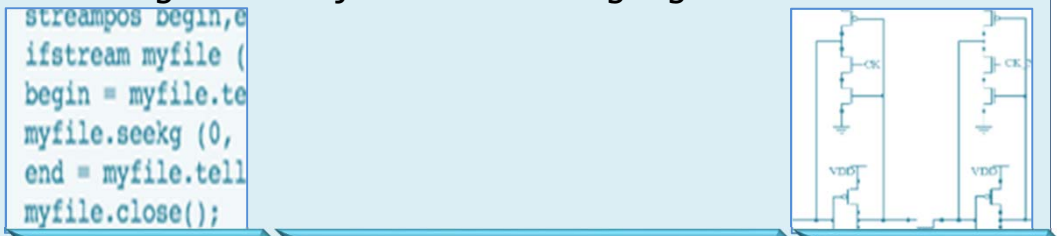
- Use of modern software engineering methods
- Automated representation translation
- Automated verification
- Reduces effort required to port design to a 2nd source foundry
- *Distributed through a government IP repository*

Raise Level of Abstraction

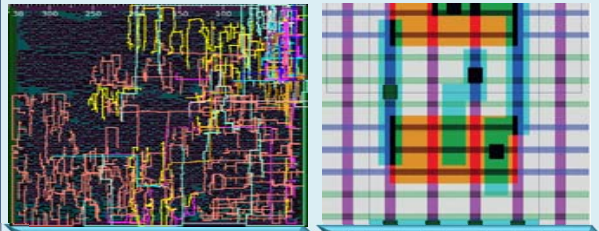
- Use existing EDA tools
- Higher level of hierarchy
- Use of generators/constructs

Object-Oriented Design (OOD) Flow

High-level object-oriented language -> Schematic

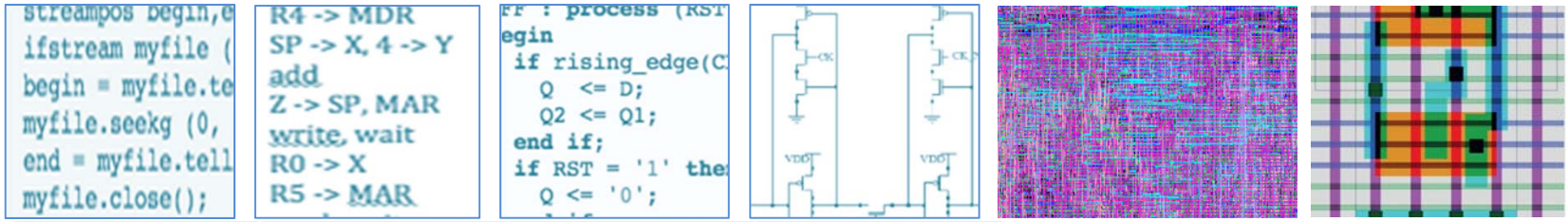


Place & Route ⇨ Layout Description



HL Code → OOD FLOW → SPICE → CELL/WIRE → OASIS

Existing ASIC Flow



HL Code → RTL → VHDL → SPICE → CELL/WIRE → OASIS

VERIFICATION

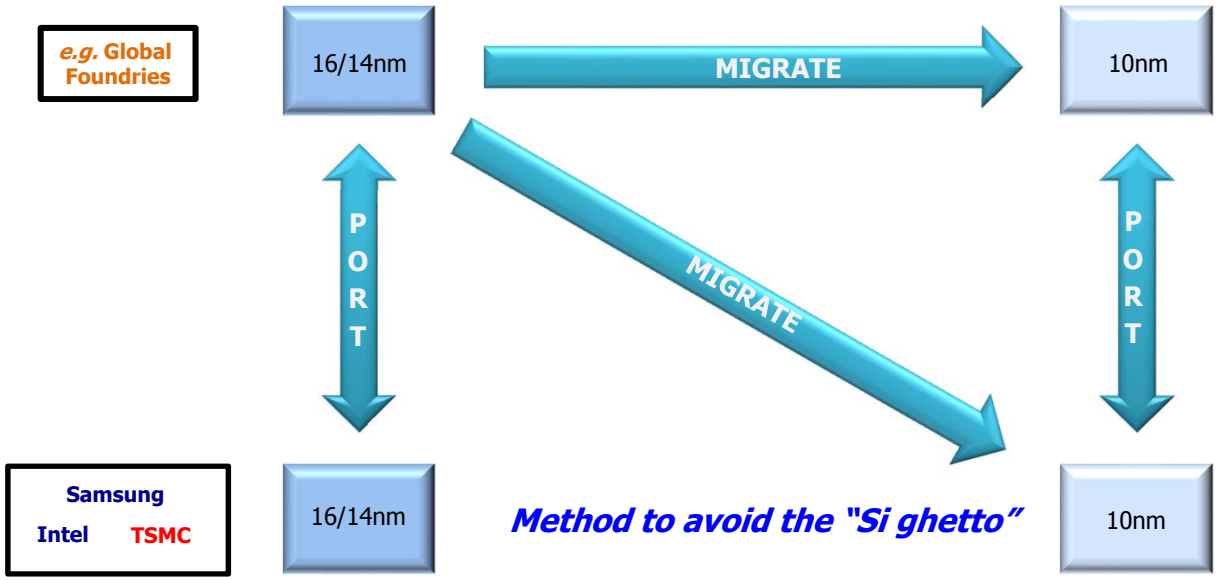
VERIFICATION

Improving Flexibility of DoD Fabrication

DESIGN | **PORT/ MIGRATE** | REPOSITORY

CRAFT aims to enable facilitated transfer of designs to multiple companies and process flows.

- Build on the CRAFT-developed Object-Oriented Design flow to develop a port/migrate flow that reduces effort by 80%
- Fabricate and analyze CRAFT macros/generators at 16nm/14nm and 10nm at other foundries to facilitate migration
- Port prototypical designs to an alternate 16nm/14nm foundry, and migrate prototypical designs to a 10nm foundry



CRAFT aims to use new design flows to ensure multiple sources of supply and reduce node migration effort by 80%

Facilitated Port/Migrate Through Use of the CRAFT OOD Flow

Current ASIC Design Flow

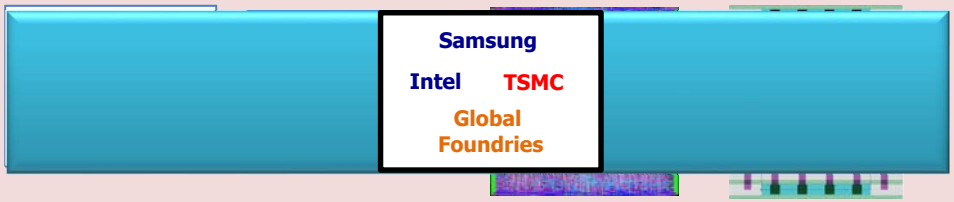
High Level description → Logical Descript'n → Gate Level Descript'n → Schematic Descript'n → Place & Route → Layout Descript'n

```
#include <iostream>
#include <fstream>
using namespace std;

int main () {
  streampos begin,end;
  ifstream myfile ("example.bin", ios::binary);
  begin = myfile.tellg();
  myfile.seekg (0, ios::end);
  end = myfile.tellg();
  myfile.close();
  cout << "size is: " << (end-begin) << " bytes.\n"
  return 0;
}
```

```
R4 -> MDR
SP -> X, 4 -> Y
add
Z -> SP, MAR
write, wait
R0 -> X
R5 -> MAR
read, wait
MDR -> Y
add
Z -> R0
```

Unique to Foundry/Node



1,000,000s of elements

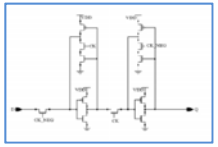
New CRAFT Design Flow

Object-Oriented Design (OOD) Flow
High level object-oriented language -> Transistor → Place & Route → Layout Descript'n

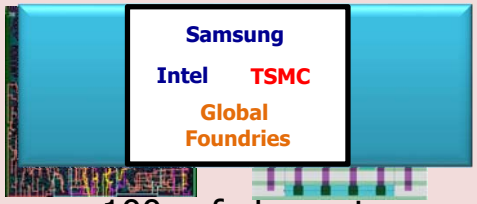
```
#include <iostream>
#include <fstream>
using namespace std;

int main () {
  streampos begin,end;
  ifstream myfile ("example.bin", ios::binary);
  begin = myfile.tellg();
  myfile.seekg (0, ios::end);
  end = myfile.tellg();
  myfile.close();
  cout << "size is: " << (end-begin) << " bytes.\n"
  return 0;
}
```

Compiled →



Unique to Foundry/Node



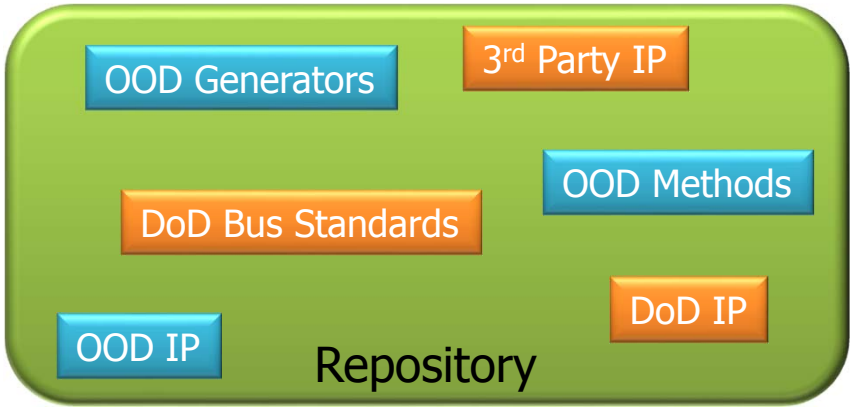
100s of elements
Stored in CRAFT repository

CRAFT aims to sharply reduce the amount of "foundry unique" work required for a design. Design foundation will be developed at a 2nd source foundry as part of CRAFT. The OOD Flow will be reused to reduce the effort to port designs.

Repository

DESIGN | PORT/ MIGRATE | **REPOSITORY**

CRAFT aims to establish location for items required for DoD users of the OOD flow



Design

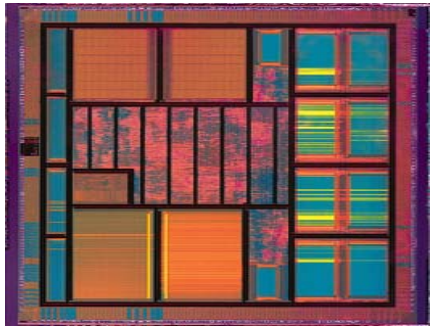


Image from Wikimedia Commons

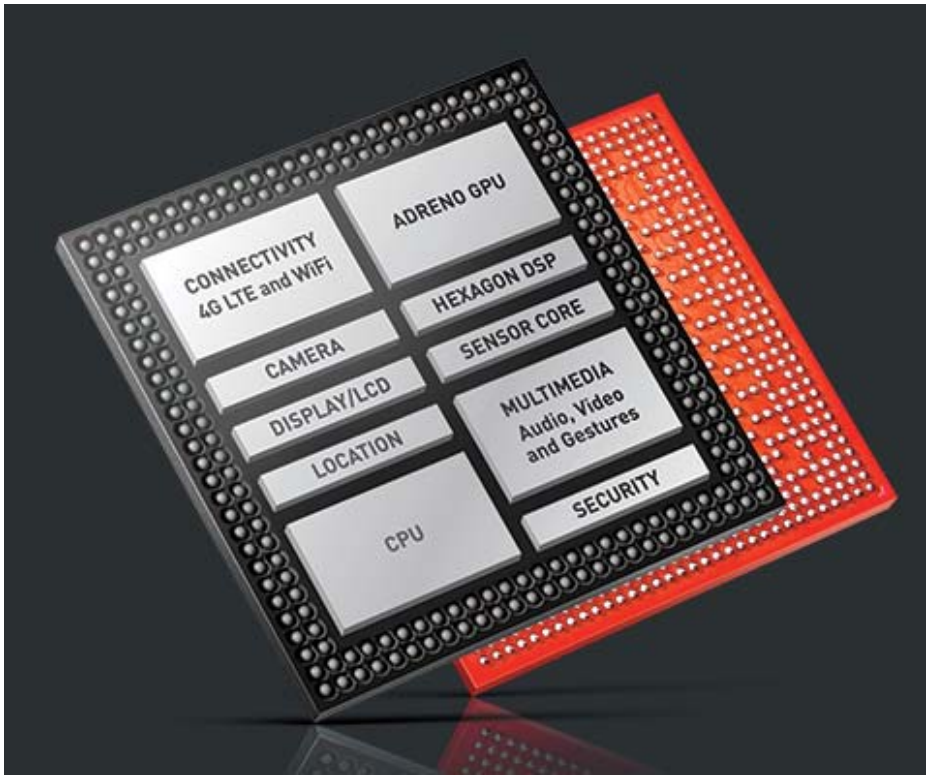
OOD flow requirements
- OOD software, tools
- OOD components
  - Generators
  - Macros
  - OOD specific IP (*eg.* RISC-V processor, Vreg, …)
- OOD examples and best practices
- Foundry-provided design rules and technology files

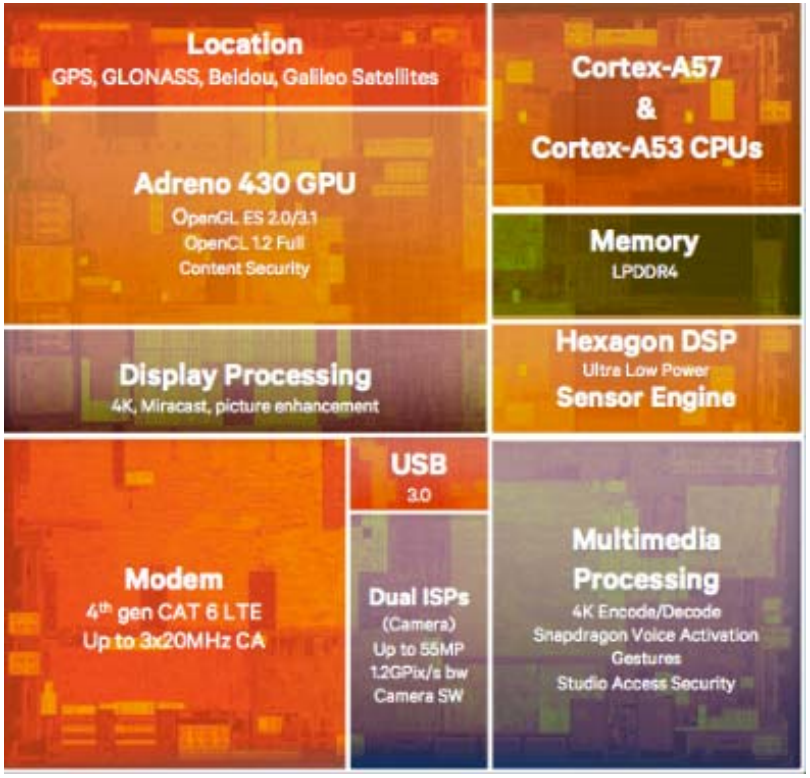
Data and models
- Foundry provided reliability
- Extended reliability (government limits)
- Device and circuit radiation response

IP
- Foundry provided IP (*eg.* SRAM bit cells, eFuse, …)
- 3rd party IP (*eg.* logic library, memory compiler, …)
- Government IP (*eg.* rad hard library, A/D, …)

CRAFT aims to establish a data location and distribution protocol to ensure efficiency through reuse of OOD flow components and methodology

Commercial Industry is Dominated by Use of IP



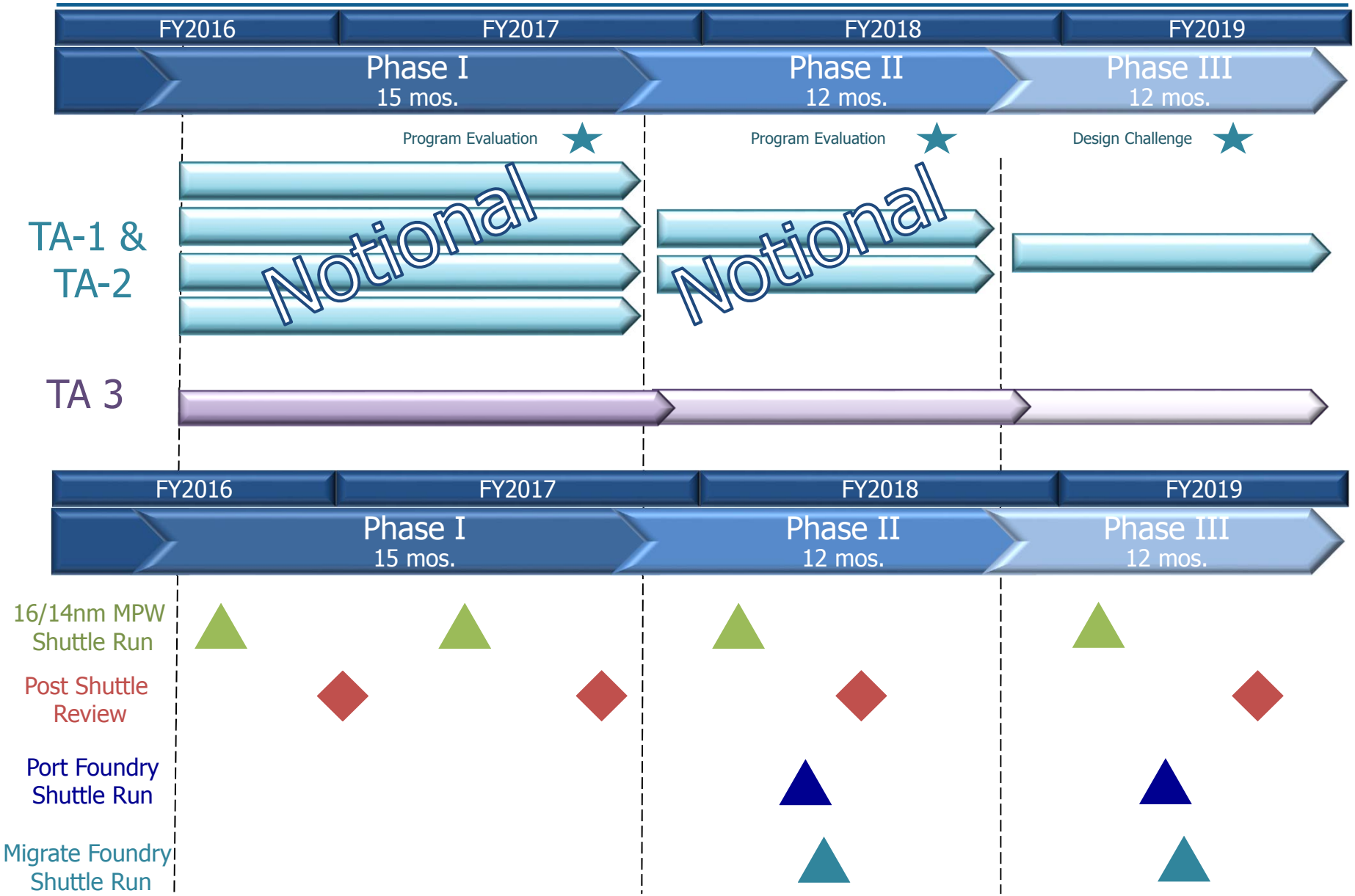


Images from qualcomm.com web site

Snapdragon is a compilation of designs from many sources

- Foundation IP (logic library, SRAM compiler, IO circuits)
- Internal IP (connectivity, DSP, GPU)
- Licensed IP (ARM CPU)
- 3rd party IP (Image processor)

CRAFT Program Plan



Proposal Guidelines

Technical Area 1 – Design

Primary goal: (BAA 15-55, page 8)

"The primary goal of TA-1 is to develop a reference design flow that can demonstrate a 10X reduction in design effort for a representative DoD custom integrated circuit design while maintaining 90% of the PAP when compared to a traditional standard-cell based design."

Design flow characteristics (BAA 15-55, pages 8-9):

- Correct by construction or heavily automated design verification over full design/process corners
- Circuit representation in a high-level language that:
  - Enables circuit architecture exploration
  - Hides process technology complexity
  - Is usable by non-experts in the field
  - Is consistent with co-development of software and hardware
- Robustness as measured by first pass design success
- Extensive reuse of design components and design effort
  - Reuse through generators or compilers
  - Definition of key high-level design macros/generators
  - Characterization of key, high-level design macros/generators
  - Seamless integration of design components provided by 3rd parties
- Applicable to design of System on a Chip (SoC) integrated circuits. That is, applicable to integrated circuits that have multiple digital, analog, mixed-signal, and memory components.
- Support for designs fabricated using the program-selected commercial FinFET foundry technology.

Technical Area 1 – Design

Critical research questions (BAA 15-55, page 9)

1. How can the design flow ensure that custom integrated circuit designs are functional and robust without extensive verification?
2. What is the set of macros or generators required to support the program goals for design efficiency across application areas?
3. How can the design flow ensure seamless utilization of existing 3rd party IP to maximizereuse and minimize verification?
4. How should the macros, generators, and IP be represented in the design flow?
5. What is the best high-level circuit representation that allows architecture exploration, hardware-software co-optimization, and design flow robustness?
6. How will you ensure that the design flow, methods, and IP developmed in TA-1 and TA-2 are effectively stored and distributed through the CRAFT repository?

Technical Area 1 – Deliverables/Phase I and II
(BAA 15-55 pages 9-10)

Phase I (15 months) – At the conclusion of Phase I, performers should have demonstrated a 5X reduction in the design effort originally required to create a design using a standard flow for a SoC of their choosing with the following characteristics:

- Logic block size of > 200k gates
- Multiple mixed signal blocks
- Multiple SRAM memory blocks
- Multiple 3rd party IP blocks

Deliverables:

- Successful simulation of chip functionality across standard corner cases
- The macros/generators sufficient to design the performer-selected integrated circuit as well as a broad range of other, similar integrated circuits
- Any unique software tools required to instantiate the design
- A fully documented reference CAD flow, including any required validation

Phase II (12 months) – At the conclusion of Phase II, performers should have demonstrated a 7X reduction in the design effort to create a full, DoD relevant design. Successful performers also will have provided sufficient documentation of the design flow to enable external, expert design groups to design full, DoD relevant designs.

Deliverables:

- Complete testing of fabricated chip functionality across standard temperature range
- Full hardware characterization documentation of an initial suite of macros/generators
- A fully documented reference CAD flow, including any required validation steps
- Definition and design of a full suite of macro/generators

Technical Area 1 – Deliverables/Phase III
(BAA 15-55 page 10)

Phase III (12 months) – At the conclusion of Phase III, performers should have defined and fully documented a complete reference flow, capable of being used to design a DARPA-selected DoD custom integrated circuit design that is fabricated and confirmed through hardware testing. Performers are also expected to provide their design flow and support to a group of independently funded teams who will design multiple DoD-specific custom integrated circuits that will be fabricated, and confirmed through hardware testing.

Deliverables:

- Complete testing of the functionality of multiple fabricated integrated circuits
- Full hardware characterization of a full suite of macros/generators
- A complete, fully documented reference CAD flow that has been exercised by multiple external design groups
- Successful completion of a design challenge using the documented reference design flow
- Plan for continued distribution, maintenance, and improvement of the reference design flow after program completion

Technical Area 1 – Metrics
(BAA 15-55 pages 15-16)

- Each performing team should have demonstrated the following rate of design of fully validated equivalent gates/day for a new, representative, custom DoD System on a Chip (SoC) integrated circuit while maintaining no less than 90% of the technology entitlement performance at power:
  - Phase I – 50k gates/engineer-day
  - Phase II- 75k gates/engineer-day
  - Phase III – 100k gates/engineer-day
- Each performing team should have demonstrated the following rate of design of analog blocks for a new, representative, custom DoD SoC integrated circuit while maintaining no less than 90% of the technology entitlement performance at power:
  - Phase I – 1.0 analog blocks/engineer-week
  - Phase II- 1.3 analog functions/engineer-week
  - Phase III – 1.5 analog functions/engineer-week
- Each performing team should have demonstrated the following reduction in design effort for a new, representative, custom DoD SoC integrated circuit when compared with a design made using the current standard cell design flow and while maintaining no less than 90% of the technology entitlement performance at power:
  - Phase I – 5X reduction
  - Phase II- 7X reduction
  - Phase III – 10X reduction
- By the end of the program, each performing team should have demonstrated the following:
  - Reduction in total design costs to less than $2M for a single, representative, custom DoD SoC design
    - Random logic block size of > 50M gates
    - Multiple mixed signal blocks
    - Multiple SRAM memory blocks
  - Top level chip verification time of less than 1 week, including DRC and LVS

Technical Area 2 – Port/Migrate
(BAA 15-55 pages 11-12)

Primary goal

The major purpose of this technical area is to ensure multiple sources of leading-edge CMOS fabrication by:

- Developing a custom integrated circuit design flow that can take an integrated circuit that was designed to be fabricated in a primary foundry/flow, and port the design to a secondary foundry/flow with less than 20% of the effort required to design the integrated circuit for the primary foundry/flow.
- Developing a design flow that will reduce by 50% the effort required to migrate a design from one technology node to a more advanced node.

Port/Migrate flow characteristics:

- Derived from the design flow developed in TA1.
- Enables porting of a representative design from a primary foundry/flow to a secondary foundry/flow with < 20% of the effort required for the original design
- Requires minimal manually-driven verification for the ported design
- Ensures first time fabrication success of the ported design
- Enables migration of a representative design from the primary foundry/flow to a more advanced flow using the primary or a secondary foundry with < 50% of the effort required for the original design.

Technical Area 2 – Port/Migrate

Critical research questions (BAA 15-55 pages 11-12)

- What hardware characterization tasks are required at the primary and secondary foundries to ensure appropriate transfer of design primitives to a new flow or a more advanced technology node?
- How can porting and/or migration be accomplished without requiring new synthesis or new pre-schematic verification?
- What simulation, hardware characterization, or verification is required to ensure equivalence of designs fabricated at the primary and secondary foundries?

Metrics (BAA 15-55 page 16)

Each performing team should have demonstrated the following:

- Porting of a custom design from a 16nm/14nm flow at the primary foundry to a same-node 16nm/14nm flow at the secondary foundry with less than 20% of the effort required for the original OOD design while maintaining the PAP of the original design:
  - Phase II: Performer-selected design
  - Phase III: DARPA-selected design
- Migration of an existing custom design from a 16nm/14nm flow at the primary foundry to a more advanced node flow with less than 50% of the effort required for the original OOD design while maintaining no less than 90% of the technology entitlement PAP:
  - Phase II: Performer-selected design
  - Phase III: DARPA-selected design

Technical Area 2 – Deliverables
(BAA 15-55 page 12)

Phase II (12 months) – At the conclusion of Phase II, performers should have designed and fabricated a full set of design primitives/macros in a secondary foundry process flow and in a more advanced foundry process node.

Deliverables:

- Design and documentation for a full set of design primitives/macros at a DAPRA-selected, secondary 16nm/14nm foundry/process flow
- Fabrication of those primitive/macros at the secondary foundry
- Design using the porting flow and subsequent fabrication of a performer-selected SoC design in the secondary 16nm/14nm foundry/process flow
- Design and documentation for an initial set of design primitives/macros in a DARPA-selected, more advanced foundry/process flow
- Fabrication of those primitive/macros using the more advanced process node
- Design using the migration flow, and subsequent fabrication of a performer-selected SoC design in the DARPA-selected more advanced CMOS technology node

Phase III (12 months) – At the conclusion of Phase III, performers should have fully characterized a full set of design primitives/macros in a secondary foundry process flow and in a more advanced foundry/process node. The performer should also have demonstrated the successful use of the porting and migration flows to design and fabricate a full, DARPA-selected, DoD SoC integrated circuit.

Deliverables:

- Design and documentation for a full set of design primitives/macros at a DARPA-selected secondary 16nm/14nm foundry/process flow
- Fabrication of the full set of primitive/macros at the secondary foundry
- Design using the porting flow and subsequent fabrication of a DARPA-selected, DoD SoC design at the secondary foundry
- Design and documentation for a full set of design primitives/macros at a DARPA-selected, more advanced foundry/process flow
- Fabrication of those primitive/macros using the more advanced process node
- Design using the migration flow and subsequent fabrication of a DARPA-selected, DoD SoC design in the DARPA-selected

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Technical Area 3 – Repository
(BAA 15-55 pages 13-14)

Primary goal

"The purpose of this task is to establish a common cyber-infrastructure approach, a trusted repository, and to define the data management plans and methods required to submit, secure, and distribute the design primitives, methods, and information required to support the goals of TA-1 and TA-2."

Repository characteristics:

- Technologies to support representation of and transformation among multiple types of data: design data, characterization data, design representations, design flow scripts and software, technology information and associated provenance for each of the above.
- Mechanisms for providing information assurance and security to this data to protect against practical threats to its authenticity, integrity, and non-reputability both while in motion and while at rest.
- An organization or process that can establish, define and manage the evolution standards for the content of the trusted repository.
- Structure for governance to receive advice on the most critical content to be included in the repository.
- Establishment of a set of data management guidelines and policies, including processes and procedures for submission of data to the repository from government and commercial entities.
- Extensive reuse of existing frameworks and software technologies for deploying cyber-infrastructure to support data-driven science and engineering, including: federated storage approaches, grid storage middleware, portals and collaboration, process capture and workflow management tools, and software for data tilling and schema management

Technical Area 3 – Repository

Critical research questions (BAA 15-55 page 14)

- What is the maximum leverage a trusted repository can have from the existing developments and technologies in cyber-infrastructure for data science? (NSF 07-28, Cyberinfrastructure Vision for 21st Century Discovery)
- What are the most efficient means to secure repository content to users?
- How can repository data be secured while maintaining maximum usability?
- What delivery methods can be instituted to reduce costs of IP and EDA tools?
- How will you ensure that 3rd party IP and EDA tools as well as the design flow, methods, and IP developed in TA-1 and TA-2 are effectively stored and distributed through this repository?

Metrics (BAA 15-55 page 17)

Each performing team should have demonstrated the following average percentage of a representative custom DoD integrated circuit die area filled with reused functions retrieved from the repository:

- Phase II – 30%
- Phase III – 50%

Technical Area 3 – Deliverables
(BAA 15-55 pages 14-15)

Phase I (15 months) – At the conclusion of Phase I, performers should have established the organization of the repository, including the basic IT infrastructure, the initial data structure, and the government/industry advisory board.

Deliverables:

- Definition of the structure of the IT infrastructure supporting the repository
- Structure for governance via a repository advisory board
- Initial definition of the format/criteria for content submission to the repository
- A plan and guidelines for submission of 3rd party IP to the repository

Phase II (12 months) – At the conclusion of Phase II, performers should have exercised the repository to support full designs.

Deliverables:

- Storage and distribution of the design elements (primitives/macros, software, methods, etc.) developed by all TA1/TA2 performers
- Summary of the repository needs as defined by the government/industry repository advisory board and users of the repository
  - Methods of use of the repository
  - Definition of the appropriate content for the repository (Design flow, IP, data)
    - Performer will not be responsible for acquisition of the content, only the definition
- Final definition of the format/criteria for content submission to the repository
- A plan for the continuation and sustainability of the repository after program completion

Phase III (12 months) – At the conclusion of Phase III, performers should have refined the organization of the repository and developed a plan for its continuation after program completion.

Deliverables:

- Storage and distribution of the design elements (primitives/macros, software, methods, etc.) developed in TA1/TA2
- Demonstration of extensive use of the repository by multiple DoD performer users
- Implementation of the plan for continuation and sustainability of the repository after program completion

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Proposal Submission Reminders

- Proposal Submission Deadline: 4:00pm EDT; Monday, 5 October 2015 (BAA 15-55, page 4)

  Do not wait until the last minute to submit!

- Volume I Page Limitations (BAA 15-55, page 28):
  - TA-1 & TA-2 Only Response: 30 pages maximum
  - TA-3 Only Response: 15 pages maximum
  - TA-1, TA-2, AND TA-3 Response: 45 pages maximum (comprised of 30 pages maximum to address TA-1 and TA-2, and 15 pages maximum to address TA-3)

Contracting Comments

- The Proposer's Day event is a mechanism to allow the DARPA PM to walk through the program goals and objectives to ensure they clearly understood. However:
  - Only the info in the BAA should be used for proposal preparation purposes.
  - If a question posed to the Gov't results in a response that differs from the BAA, the BAA will be amended and typically noted in advance in the FAQ.
- The Government may select for negotiation all, some, or none of the proposals received.
- The Government may accept proposals in their entirety or select only portions thereof.
- The program will be funded with 6.1 and/or 6.2 funds. This means that work performed by schools will be fundamental (prime or sub).
- All award instrument types are available (contract, grant, cooperative agreement, and Other Transaction.

Contracting Comments (Continued)

- There are no restrictions in the BAA on who can propose (foreign participants are permitted)
- The program is not classified and involves no classified information.
- All proposers MUST adhere to the page limitation for technical proposal.
- Proposers MUST submit proposals on time
  - Late proposals - no matter how late - will not be reviewed.
  - Late is Late!!!!
- Full subcontract cost proposals are required. ROMs are not sufficient
- If only a ROM is provided, the proposal may be deemed non-compliant and not reviewed.
- To receive a cost type contract you must possess a DCMA approved cost accounting system. If you are seeking such an award instrument, and don't have an approved cost accounting system, see instructions in the BAA.
- All communications between now and receipt of select/non-select letters will be conducted primarily via the BAA email address and FAQ.

CRAFT Summary

- Vision

  "To sharply reduce the barriers to DoD use of custom-integrated circuits built using leading-edge CMOS technology while maintaining the high level of performance at power promised by this technology."

- Method
  - Fund proposers to develop a new "OOD Flow" that reduces design/verification effort for a generic DoD SoC design by 10X
  - Fund proposers to utilize the "OOD Flow" that reduces design/verification effort to port/migrate a design by 5X and 2X respectively
  - Fund a proposer to establish a Repository to enable a sharp increase in the reuse of methods and IP in DoD SoC designs
  - Schedule, support, and plan multi-project fabrication runs using commercially available FinFET technology

- Schedule
  - BAA release – 8/17/15
  - Proposals due – 10/5/15
  - Program kickoff – February/March 2016

DARPA Wants to "Ride the Wave" to Exciting Places!

The "Wave" (smartphone market example)

- Global consumers
- > $265B market (global revenue in 2013)*
- Drives leading-edge CMOS technology
- Requires digital, analog, and RF advances
- Burdened by large SoC design investments
- Pays for large, production wafer volumes
- "Generates" the power of the wave

* Statista.com website

Frank Kovalchek from Anchorage, Alaska, USA

U.S. Marine Corps Photo

The "Surfer" (DoD system development/deployment)

- Global suppliers
- < $1.5B market (US Government business in 2013)**
- Utilizes commercially driven CMOS technology
- Leverages digital, analog, and RF advances
- Drives new, boutique design/architecture approach
- Pays for low wafer volumes
- "Utilizes" the power of the wave

** IC Insights "IC Market Drivers 2014 Update"

How Do I Ask Questions?

- Send any questions or requests for clarification to the CRAFT BAA Coordinator (DARPA-BAA-15-55@darpa.mil), per the instructions found on page 42 within BAA 15-55:

- Please provide the following information:
  - User name
  - User email address
  - User phone number
  - User organization
  - Brief description of question
  - Page reference(s) within the BAA

- URL on FedBizOpps: http://ow.ly/QZPzX

www.darpa.mil