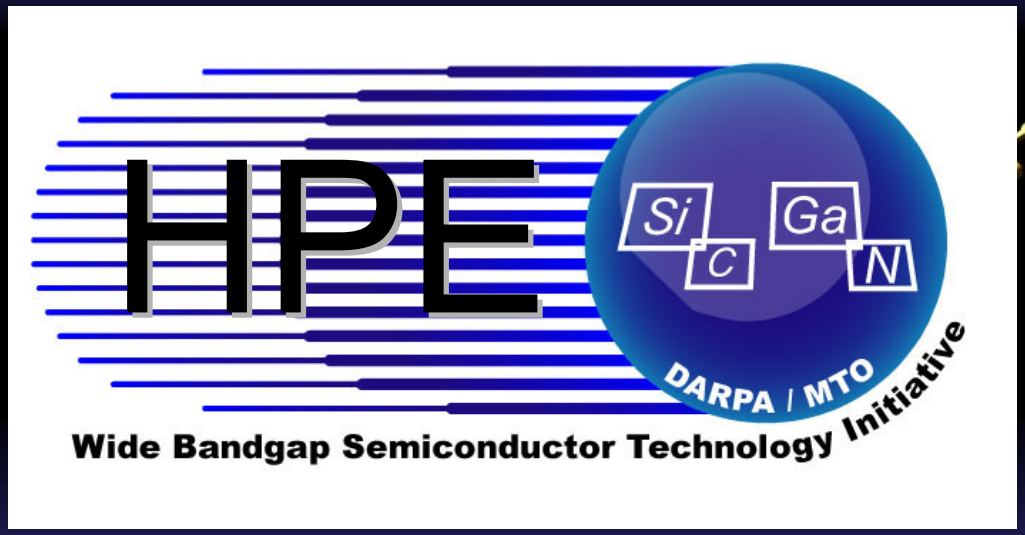
Wide Bandgap Semiconductor Technology: High Power Electronics Phase II and III



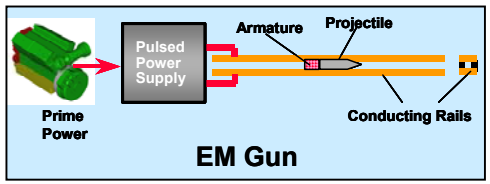
Dr. John C. Zolper, Deputy Director/PM

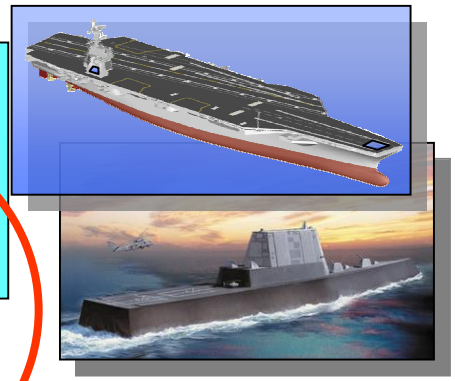
Industry Day

16 June 2004

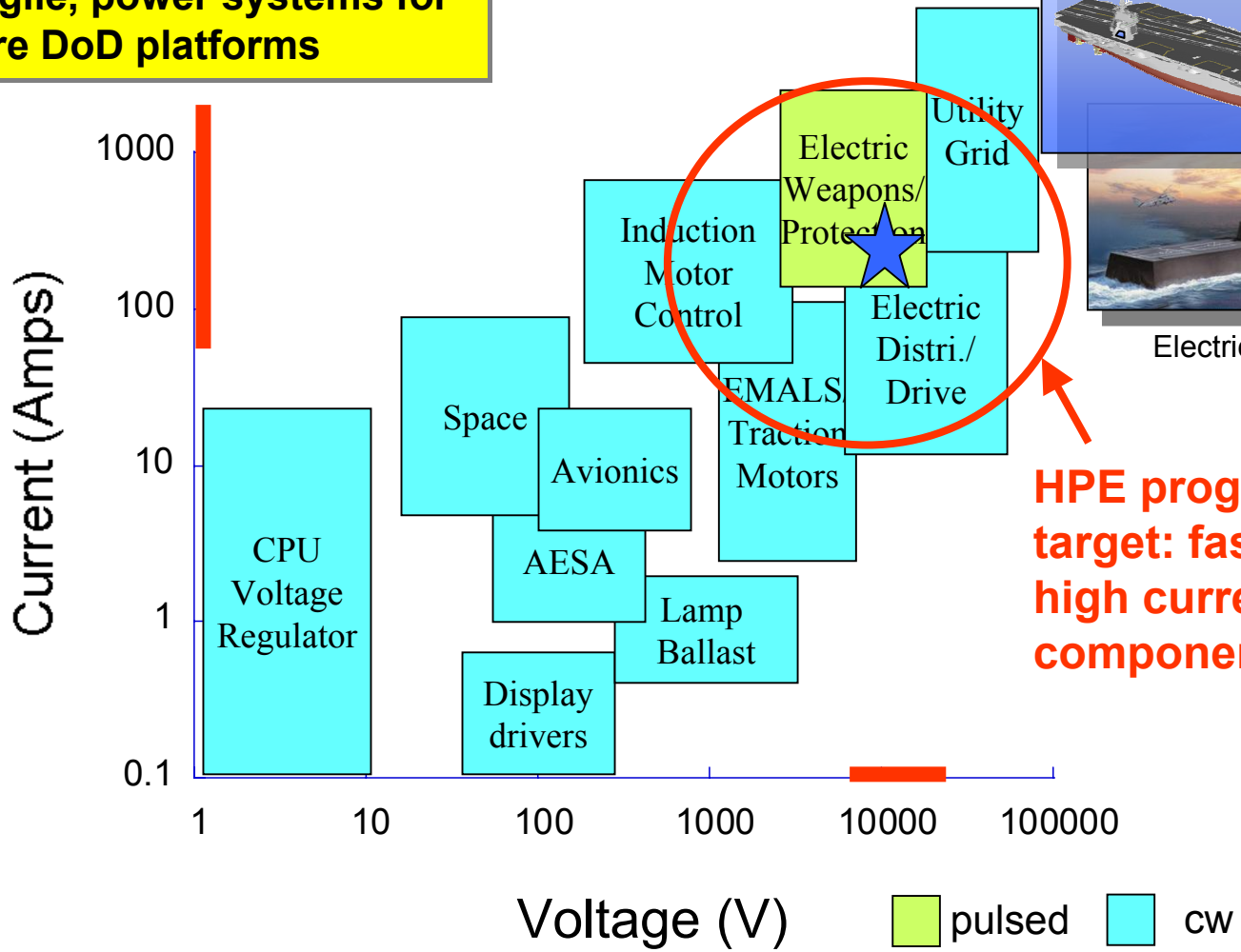
HPE Program Goal

Realize a new class of high performance MW-class solid state power devices to enable efficient, compact, agile, power systems for future DoD platforms



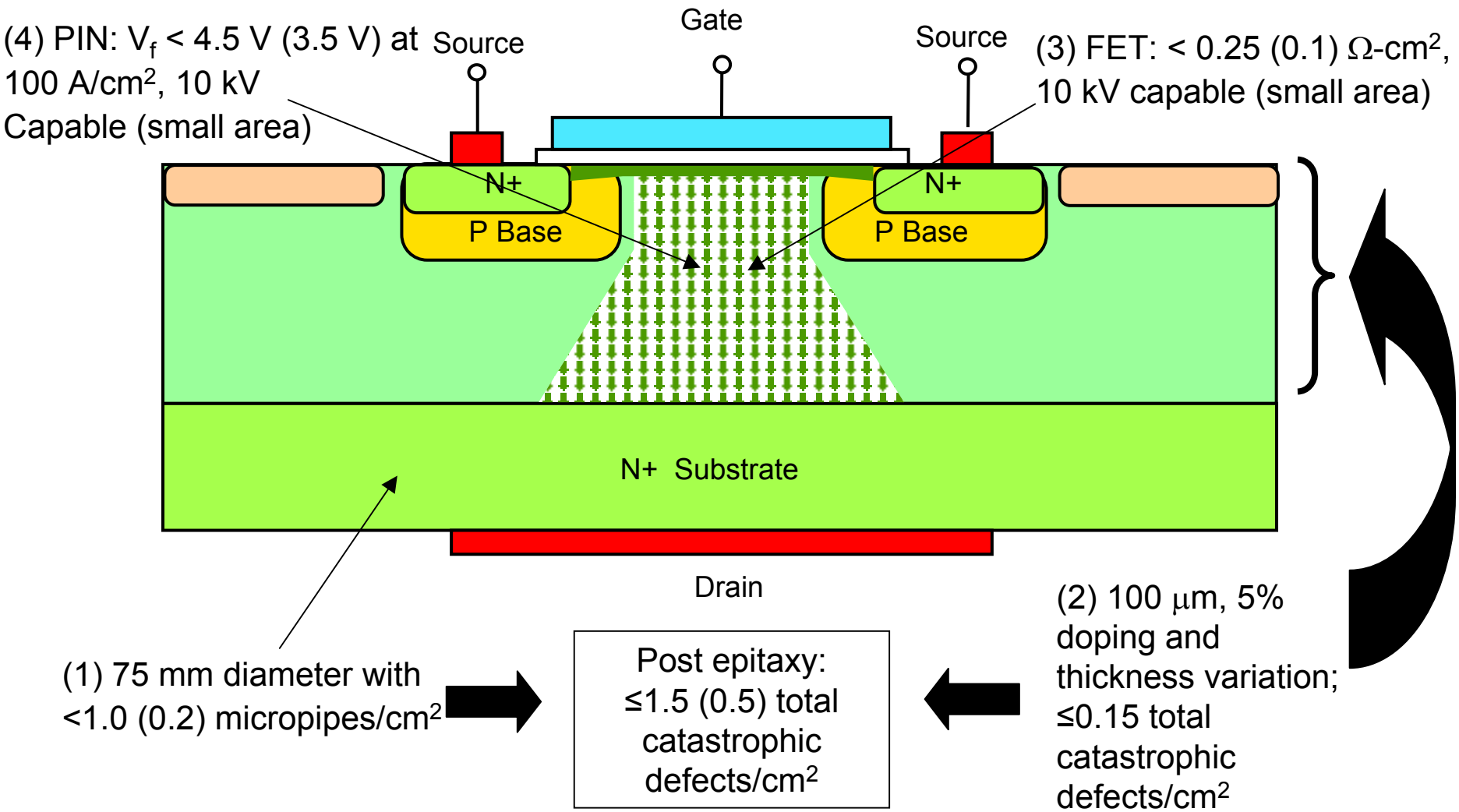


Electric Warship



HPE program target: fast, low loss, high current, ≥10 kV components

Phase I: Establish Material Capability



SiC Power Transistor

Phase I Metric Status

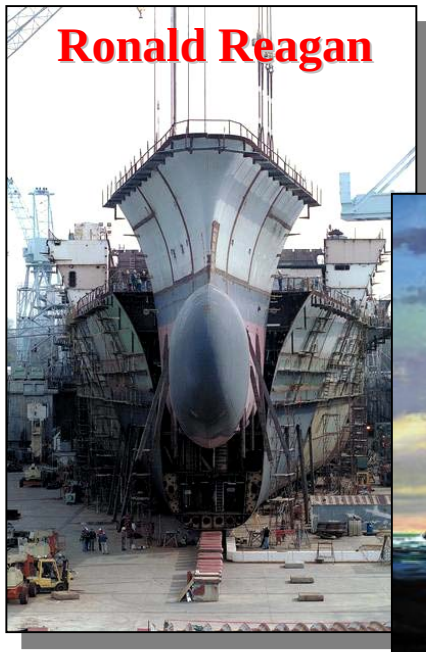
As of June 2004

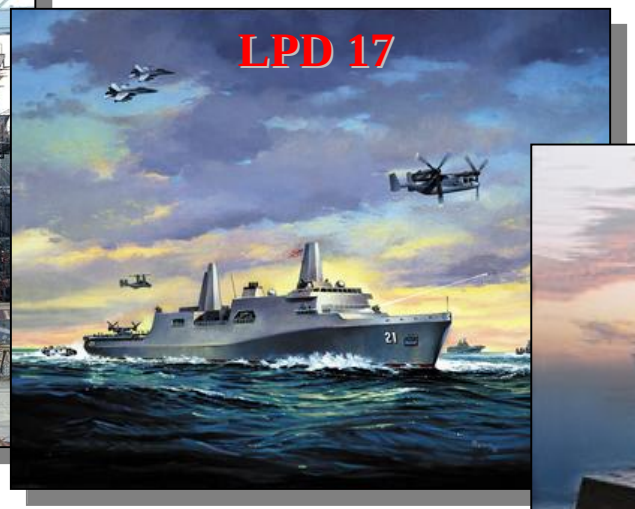
metric	Program start	Execution phase I GNG	June '04	Phase I End Goal
1. SiC n-type substrate mircopipe density (per cm^2)	15	**1.0**	**0.19**	**0.2**
2a. Thick epi doping and thickness uniformity	N/A	**100 μm ±5%; doping ±5%**	100 μm ±1.6%; doping <5%	150 μm ±5%; doping ±5%
2b. Total electrically active defects after epi (per cm^2)	N/A	**Total ≤ 1.5**	1.4	Total ≤ 0.5
3. MOS on-state performance for 10 kV blocking (Ω-cm^2)	N/A	**0.3**	<0.25	0.1
4. Bipolar on-state performance (V_f) for 10 kV blocking (V at 100 A/cm^2)	>6	**5.0**	3.8	3.5

Future Ship Systems

Every ship in the Navy is space and weight critical

Future ships will be all electric

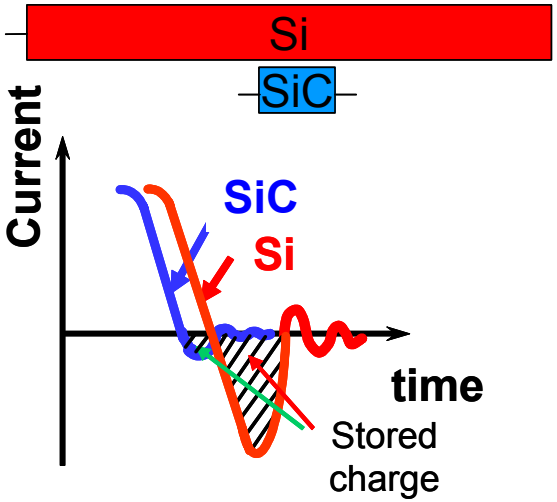




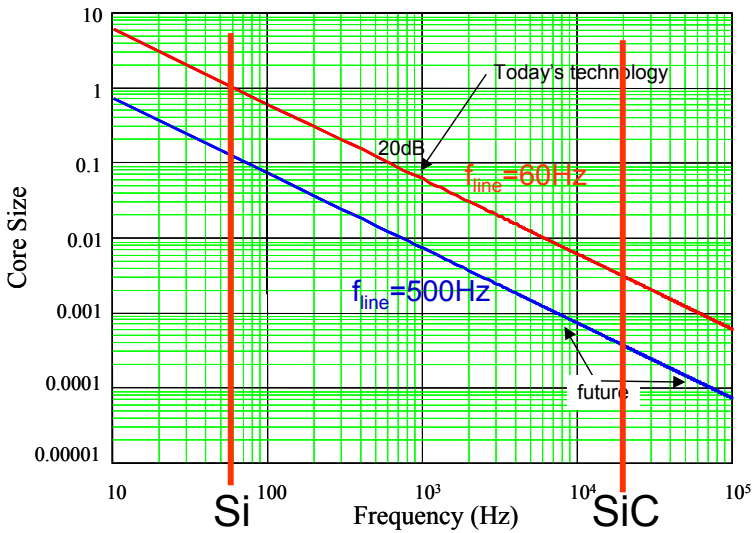
<u>Desirable Attributes</u>

- **More Efficient Power control**
- **Smaller size and lighter weight power systems**
- **Increased system flexibility**

SiC Power Electronics
Enabler for Electric Warship



Si vs SiC diode switching



Transformer Size Decreases with Frequency

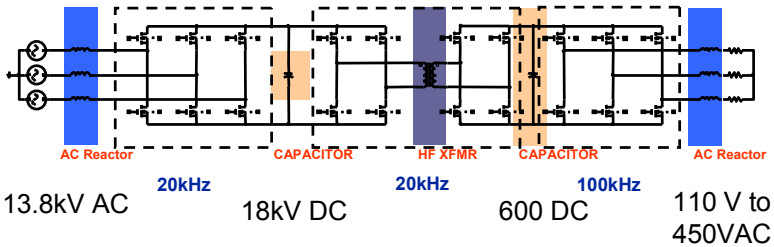
- **SiC Power Transistors**
  - Lower on-resistance
  - Lower switching loss
  - Higher switching frequency
  - High temperature operation
- **System Impact**
  - Reduced transformer size and weight
  - Dynamic power management for fight through capability
  - Flexible load management

13.8 kV – 450 V Solid State Power Substation (SSPS)

Conventional Approach:
Low Frequency Transformer (analog)

Transformer:
- 2.7MVA
- 13.8kV/450V 60Hz
- **6 tons/each**
- **10 m³/each**
- **fixed, single output**

SiC-based Solid State Power Substation (digital)



Solid State Power Substation (estimated):
- 2.7 MVA
- 13.8kV/450V 20 kHz
- **2.7 tons/each***
- **~4 m³/each***
- **multiple taps/outputs**

* Initial estimates

Additional performance features of SiC SSPS
- Precise voltage regulation (sag, flicker, harmonics)
- Operates at Unity Power Factor to source (effective 20% increase in useable power)
- Fast fault detection, protection and restoration (potential to eliminate circuit breaker)
- Easy energy storage
- Enables DC distribution

Solid State Power Substation (SSPS)

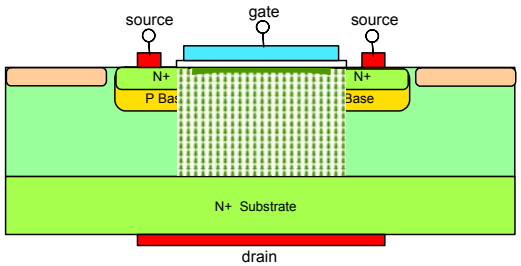
- 2 studies with SiC devices
  - 115 kV stepped down to 13.8 kV (utility application)
  - 13.8 kV stepped down to 4160/450 V
- SiC impact on SSPS
  - Estimated 50% or more reduction in weight*
  - Estimated 60% or more reduction in volume*
- Additional features of SiC SSPS
  - Precise voltage regulation (sag, flicker, harmonics)
  - Operates at Unity Power Factor to source
  - Fast fault detection, protection and restore (circuit breaker may be eliminated)
  - Easy energy storage
  - Enables DC distribution
  - Reduction of breakers and motor controllers

* Initial estimates

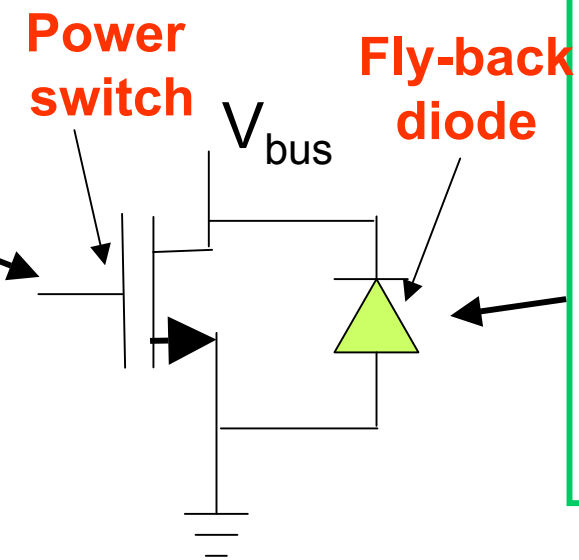
Strategy for HPE Phase II/III: Power Circuit Elements

Phase II

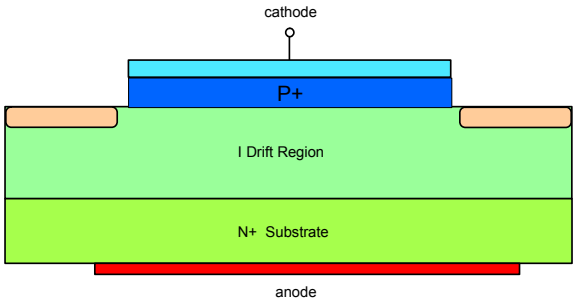
10 kV Switch Func (J, V, freq)



MOSFET: BV, R_{on}, I_{on}, Freq



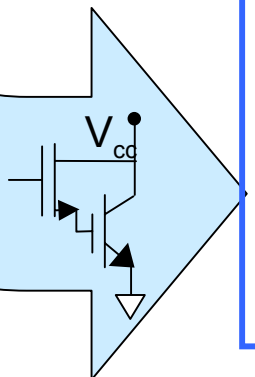
10 kV Diode: BV, V_f, I_{on}, freq.

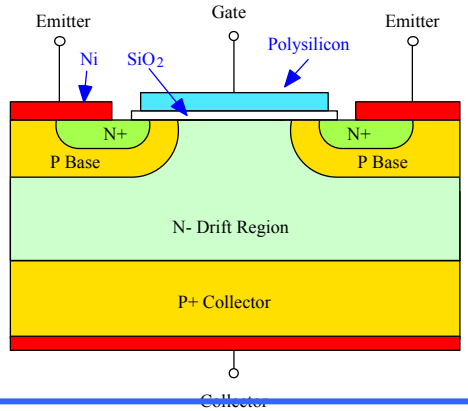


PIN diode

Phase II

Phase III: Combine MOSFET and PIN for high voltage and current





15 kV MOS Gated Bipolar Transistor

BAA 04-28 Areas of Interest

- Solid State Power Substation topology
- Materials Extension driven by device requirements
- Diode (PIN)
- Switch
  - MOSFET
  - IGBT
  - Other? (must be clearly justified)
- Packaging and Modules
  - Diode, Switch, Switch/Diodes module
- Reliability
- Technology Extensions

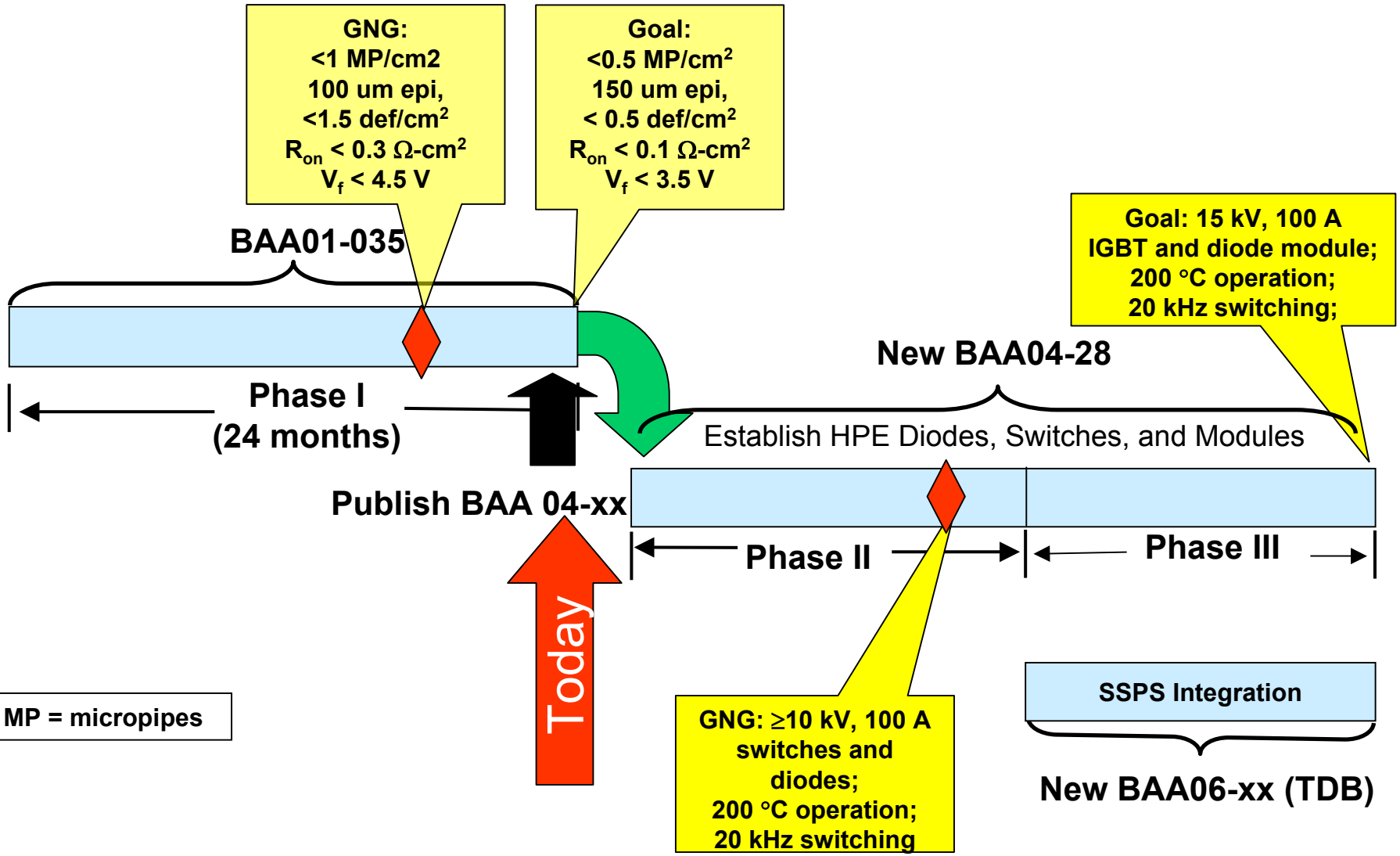
Development coupled to system need

Program Strategy

- Transition from small area hero demonstrations to large area total power device production
- Multiwafer process lots
- Statistical performance and wafer maps
- Yield targets
- Reliability assessment
- Packaged deliverables
- Study targeted DoD applications
- Establish component suppler for any power system integrator

DARPA's HPE Potential Program Schedule

Establish Materials



Potential Program Metrics

- BAA cites representative metrics
- Offerers must clearly describe how metrics will be met or …..
- Propose alternative metrics with clear justification.

PIN Diode

Table I: Representative die level Go/No-Go Metrics for PIN Diodes.
All metrics must be met simultaneously unless otherwise noted.

Metric	Phase II GNG	Phase III Program Goal
T_j (°C)	200	200
BV (V)[1]	≥10,000	≥ 15,000
V_f (V)[2]	≤4.25	≤ 4.5
I_{on} (A) (DC, discrete die)	≥45	≥90
Switching frequency (Hz)[3]	20,000	20,000
Die Yield (%)[4]	≥ 30	≥ 50

[1] Reverse Blocking Voltage at 1mA/cm^2 after 100 hr at 80% of target BV at 200 °C.
[2] Vf at 100 A/cm^2 from 0 °C to 200 °C and after forward bias stress of 100 A/cm^2 for 100 hrs.
[3] Diode reverse recovery must support 20 kHz operation in a switch/diode module.
[4] Wafer yield based on 6 wafer lot with die level metrics as shown.

MOSFET (or equivalent)

Table II: Representative die-level Go/No-Go metrics for power MOSFET.
All metrics must be met simultaneously unless otherwise noted.

Metric	Phase II GNG
T_{jmax} (°C)	200
BV (V)[1]	≥10,000
R_{on} (ohm-cm^2)	≤0.25
V_{th} (V)[2]	5 ± 0.5
I_{on}(max) (A) (discrete die)	≥18
Switching frequency (Hz)	20,000
Die Yield (%)[3]	≥ 30

[1] Reverse Blocking Voltage at 1 mA/cm^2 and V_g = 0V after 100 hr at 80% of target blocking voltage at 200 °C.
[2] Vth defined as the voltage where the current drops to 0.001 of the maximum I_{on} for V_{DS} > V_{knee}. V_{th} must be stable ($\Delta V_{th} \leq 0.2$ V) over 100 hours with 80% drain voltage rating and 100% gate voltage rating; and switching at 100% rated current with 50% duty cycle.
[3] Wafer yield based on 6 wafer lot with die level metrics as shown.

IGBT (or equivalent)

Table III: Representative Go/No-Go metrics for SiC IGBT.
All metrics must be met simultaneously unless otherwise noted.

Metric	GNG
T_{jmax} (°C)	200
BV (V)[1] (Vce)	≥15,000
V_f (V)[2]	≤ 5
V_{th} (V)[3]	5 ± 0.5
I_{on}(max) (A) (DC, discrete die)	≥55
Switching frequency (Hz)	20,000
Die Yield (%)[4]	≥ 50

[1]Reverse Blocking Voltage at 1 mA/cm^2 and Vg =0V at rated blocking voltage after 100 hr at 200 °C.
[2]Vf at 100 A/cm2 at 200 C and after forward bias at 100 A/cm^2 for 100 hrs.
[3] Vth defined as the value of V_{CE} where the current drops to 0.001 of I_{on}(max) with for VCE >> Vknee.
V_{th} must be stable ($\Delta V_{th} \leq 0.2$ V) over 100 hours with 80% drain voltage rating and 100% gate voltage rating; and switching at 100% rated current with 50% duty cycle.
[4] Wafer yield based on 6 wafer lot with die level metrics as shown.

Module

Table IV: Representative Go/No-Go metrics for complete modules. All metrics must be met simultaneously unless otherwise noted.

Metric	Phase II GNG	Phase III Program Goal
T_{jmax} (°C)	200	200
BV (V)[1]	≥ 10,000	≥15,000
I_{on} (A)[2]	110	110
Switching Frequency (Hz)	20,000	20,000
Configuration	MOSFET and PIN diode half bridge module	IGBT and PIN diode half bridge module

[1] Voltage at 1 mA/cm^2 and Vg =0 V after 100 hr at rated blocking voltage at 200 °C.
[2] DC current rating.

Summary

- Phase I established material viability
- Phase II/III will exploit material in high total power devices for real DoD applications (e.g. High voltage distribution for Naval ships).
- BAA addresses component developments to support circuit prototype demonstration
- BAA requests white papers and then proposals for delivery of robust, packaged, high total power switches and diodes.

Collaboration website

All Industry Day presentations will be posted on the BAA Teaming Site at the following website following the meeting.

http://www.davincinetbook.com/teams/login.asp

BAA posted at:

http://www2.eps.gov/spg/ODA/DARPA/CMO/BAA04%2D28/Attachments.html

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