



---

## A Strategic Thrust of the Center for Bio-Optoelectronic Sensor Systems

**DARPA Optoelectronic Center Kickoff Meeting**

Dana Point, California

November 8, 2000

Presented by

K.C. Hsieh

Department of Electrical and Computer Engineering

University of Illinois at Champaign-Urbana

Urbana, IL 61801

Tel: 217-244-1806, Fax: 217-244-6375, Email: [k-hsieh@uiuc.edu](mailto:k-hsieh@uiuc.edu)

# Heterogeneous Integration/Information Fusion



## Bio-Optoelectronic Sensor Systems center strategic thrusts

- ❖ Vapor Phase Sensors
- ❖ Liquid Phase Sensors
- ❖ **Heterogenous Integration / Information Fusion**

## Heterogenous Integration / Information Fusion thrust co-PIs

Research Topic	Investigators	Institution
1. Fabrication of optical MEMS, spectrometer, and FTIR.	C. Chang-Hasnain K. Lau	University of California at Berkeley
2. Integration of emitter, detector and spectrometer for vapor phase sensors.	M. Feng K. C. Hsieh	University of Illinois
Integration of liquid phase sensors	M. A. Brooke N. M. Jokerst S. E. Ralph	Georgia Institute of Technology
Information fusion and bio-agent identification	Z. P. Liang	University of Illinois

# Heterogeneous Integration/Information Fusion



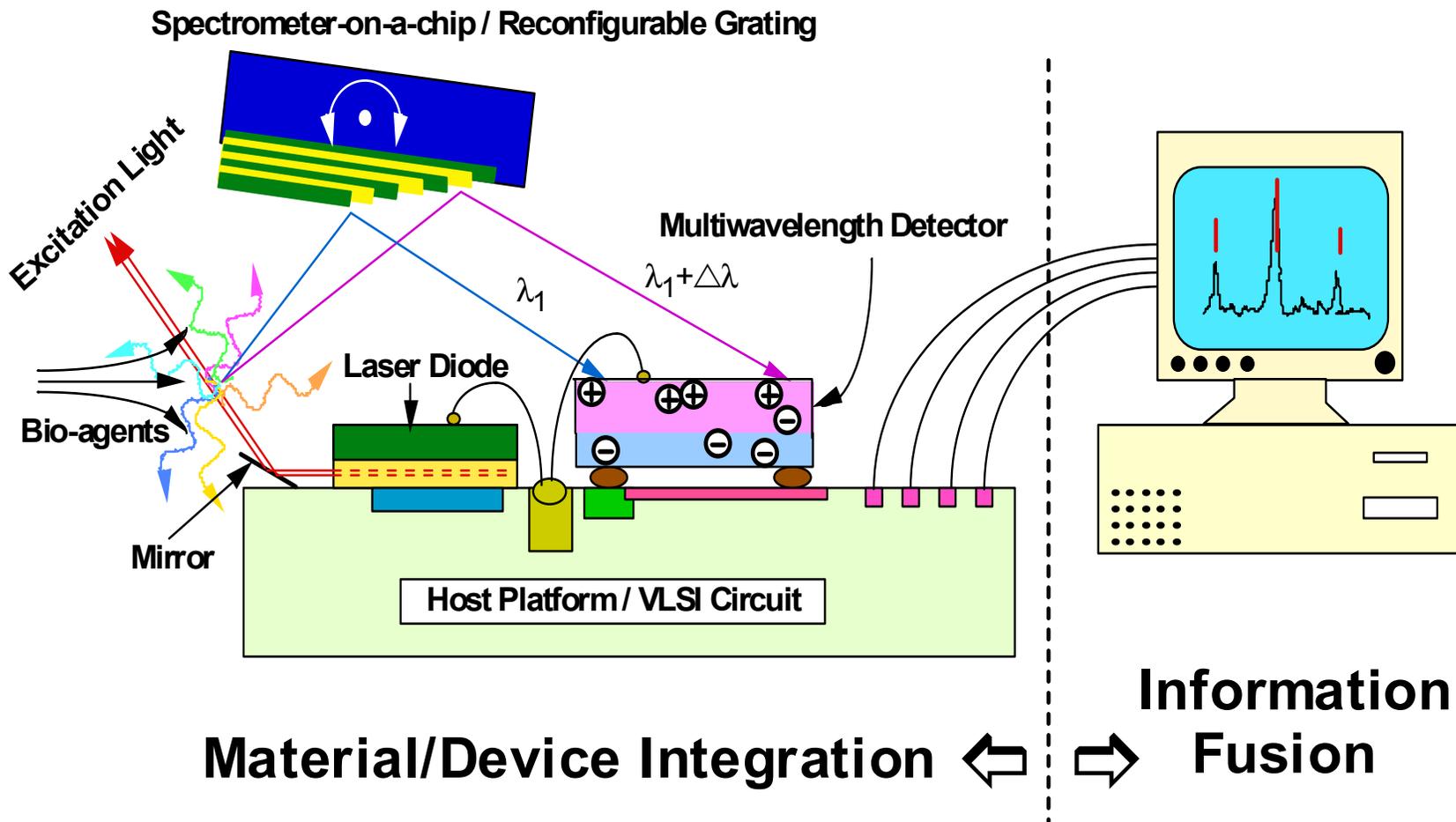
## Objective:

- ❖ Develop heterogeneous material/device integration using wafer fusion, bump bonding, thin film transfer and MEMS technology for packaging and assembly of components for detecting bio-agents optoelectronically.
- ❖ Establish spectral database and identify spectral responses of bio-agents.

## Approach:

- ❖ Vapor phase sensor
- ❖ Liquid phase sensor
- ❖ Information fusion

# Biological/Biochemical Sensing System Integration

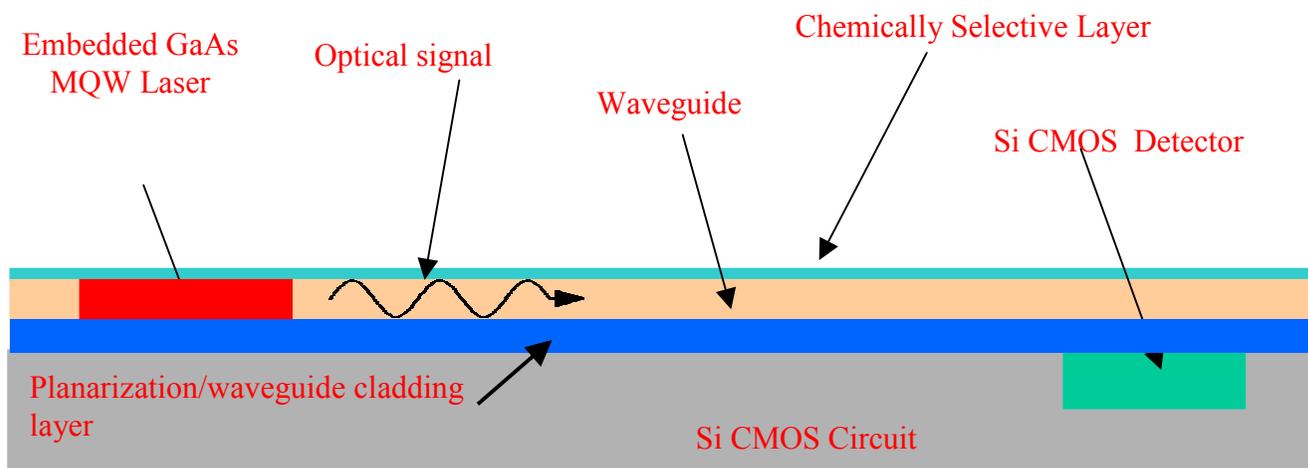


# Heterogeneous Integration of Optoelectronics onto Si CMOS Circuits



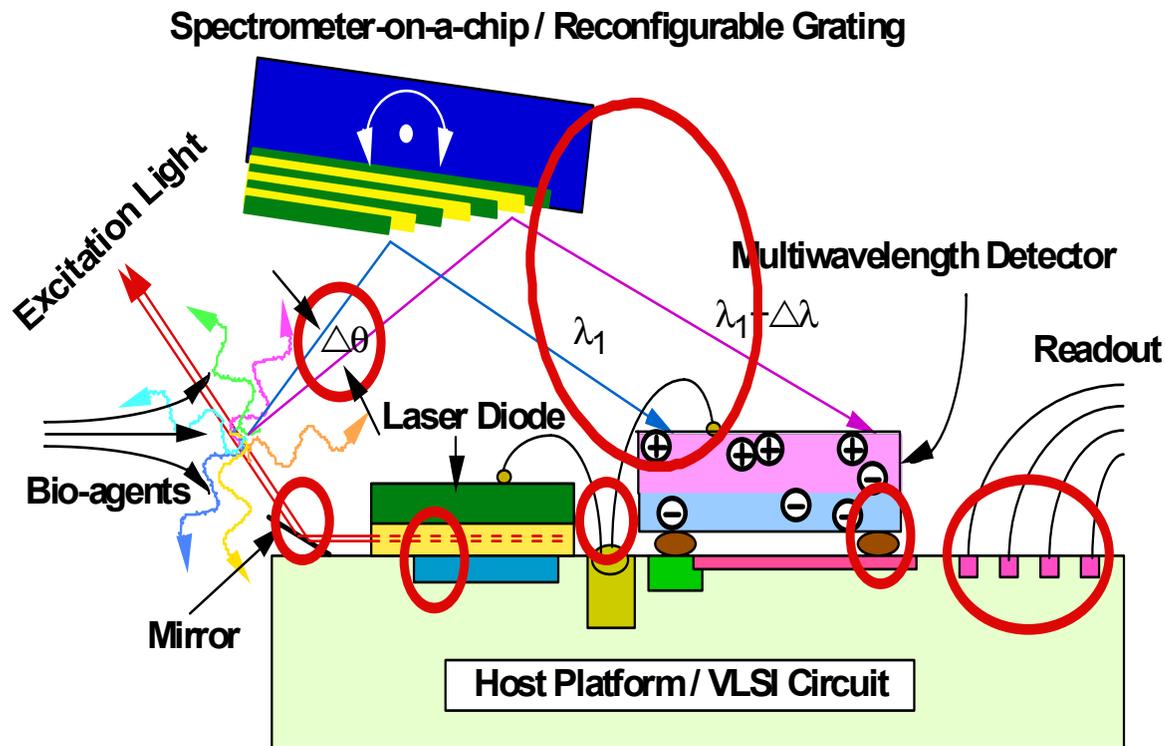
**N. Jokerst, M. Brooke, S. Ralph (Georgia Tech);**

**Objective: To design and fabricate interferometric biological and chemical sensors using heterogeneously integrated GaAs-based emitters and waveguide differential sensors integrated in three dimensions (3D) on top of Si CMOS VLSI detector and signal processing circuitry.**



Embedded laser, waveguide sensor heterogeneously integrated onto Si CMOS VLSI and detectors

# Sub-system Integration



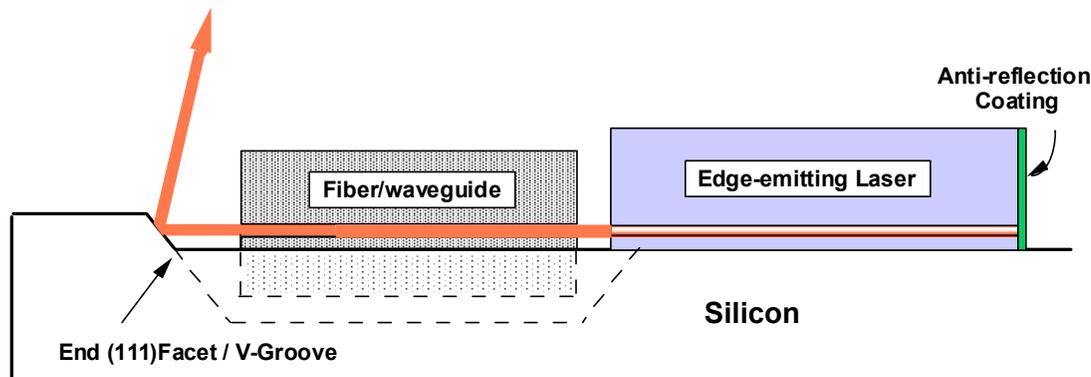
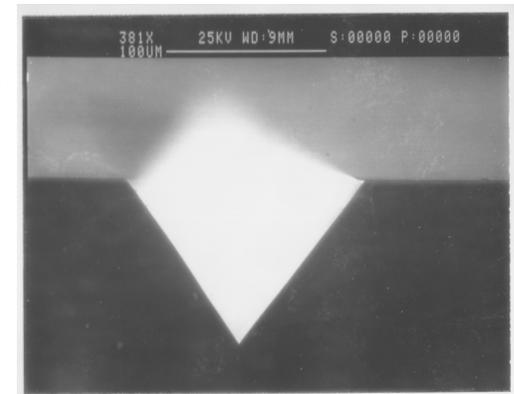
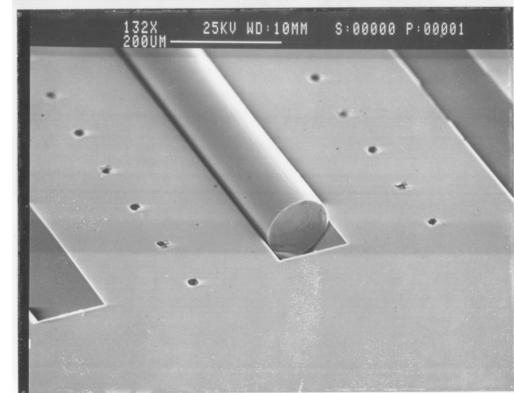
## Vapor Phase Sensor

- emitter/platform
  - wavelength, substrate, heat
- excitation light/spectrometer
  - mirror, fiber waveguide, luminescence/absorption, spatial/spectral resolution
- spectrometer/detector
  - wavelength dispersive, FTIR, Raman, luminescence/absorption, multichannel/multispectral
- detector/platform
  - front/back illumination, electrical/optical communication selection
- power (platform, emitter, detector, reconfigurable grating)
- VLSI circuit/ readout

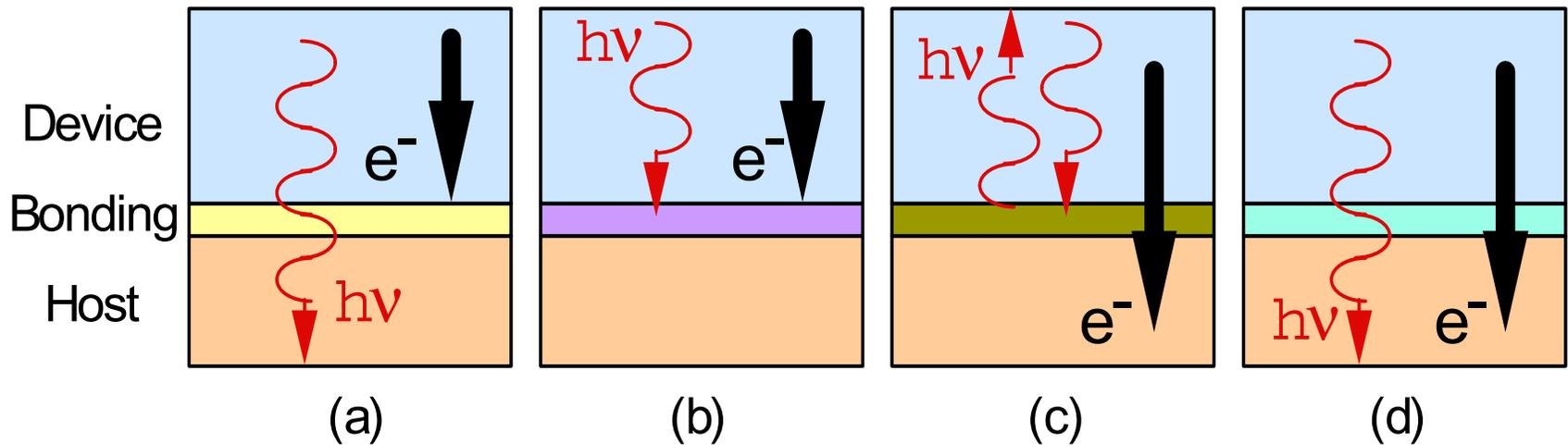
# Coupling Between Excitation Light and Spectrometer



- Anisotropic etching for V-grooves and  $\{111\}$  end facets.
- Multimode optical fiber guiding mid IR to the mirror facets or directly to the spectrometer.
- Angle-adjustable optical MEMS mirror directing excitation light to bio-agents.



# Electrical/Optical Bonding Configurations



Wide-gap insulator

Metal on insulator

Metallic compound

Wide-gap conductor

# Heterogeneous Material/Device Integration



## A. Monolithic Heteroepitaxy

Technology	Strength	Challenge
Large-wafer strained layer epitaxy or metamorphic growth	<ol style="list-style-type: none"> <li>1. Economic for single device structure</li> <li>2. Advantageous planar processing</li> </ol>	<ol style="list-style-type: none"> <li>1. Defect formation beyond critical thickness</li> <li>2. Incremental multilayer graded structure</li> <li>3. Matrix hardening limits alloy composition</li> <li>4. Complete strain relaxation requires thick epitaxial film</li> </ol>
Selected area epitaxy	Integration of multiple device structure	<ol style="list-style-type: none"> <li>1. Same as above</li> <li>2. Nonuniform lithographic-pattern dependent growth</li> </ol>

## B. Hybrid Integration

Technology	Strength	Challenge
Direct wafer bonding / Twist-and-bond compliant substrate	<ol style="list-style-type: none"> <li>1. Free intergration of dissimilar materials</li> <li>2. Strong interfacial bonding with low threading dislocations</li> <li>3. Strain-tolerant large misfit heteroepitaxy</li> </ol>	<ol style="list-style-type: none"> <li>1. Misorientation dependent contact resistance</li> <li>2. Thermal stress in thick layers</li> <li>3. Limited flexibility in multiple small area bonding for integration</li> </ol>
Thin film transfer	Flexible hybrid device integration	<ol style="list-style-type: none"> <li>1. Thin film handling and transferring</li> <li>2. Alignment for pick-and-place assembly</li> </ol>
Flip-chip bump bonding	<ol style="list-style-type: none"> <li>1. Flexible hybrid device or chip integration</li> <li>2. High resolution passive self-alignment</li> <li>3. Enhanced I/O capacity</li> </ol>	<ol style="list-style-type: none"> <li>1. Exclusive use for device/chip integration</li> <li>2. Contact pressure needed for bonding</li> <li>3. Bump size vs. device dimension</li> </ol>
Microsystem integration (MEMS)	<ol style="list-style-type: none"> <li>1. Passive components / Active actuator</li> <li>2. 3-D components integration</li> </ol>	Mesophase physics and mechanical properties need to be explored

# Material/Device Integration

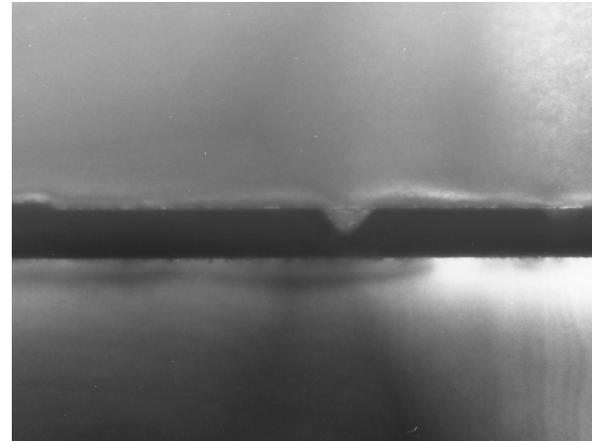


## Wafer-to-Wafer

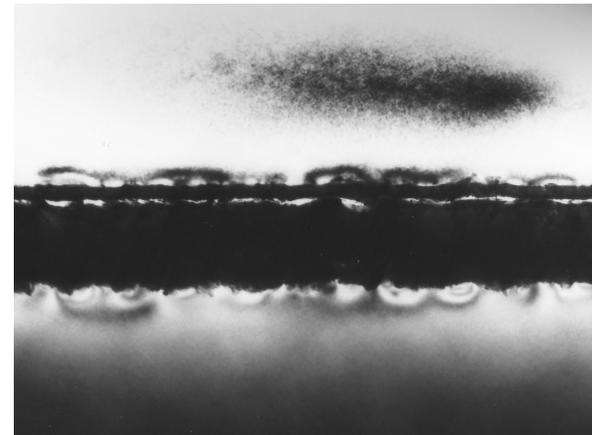
- ◆ **Direct Wafer Bonding**  
GaN, GaP, GaAs, InP, GaSb, Si
- ◆ **Metallic Bonding Agent**  
GaAs/AuGe/GaAs  
GaAs/(Pd,Zn)/Si
- ◆ **Non-metallic Bonding Agent**  
GaAs/SOG/GaAs

## Device-to-Device

- ◆ **Solder Ball Grid Array**  
Si/SiO<sub>2</sub>/Solder/SiO<sub>2</sub>/Si;  
SiO<sub>2</sub>/Solder/SiO<sub>2</sub>
- ◆ **Thin Film Transfer**
- ◆ **MEMS Technology**

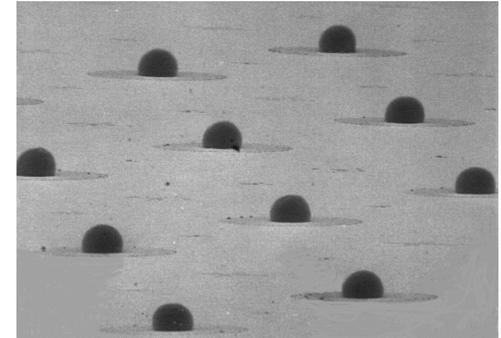
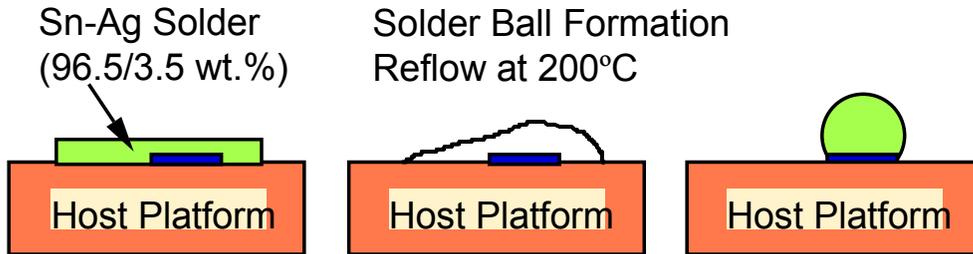


GaAs  
(AuGe)  
GaAs

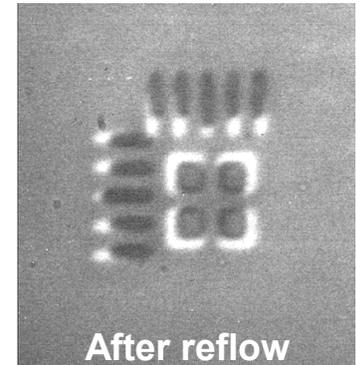
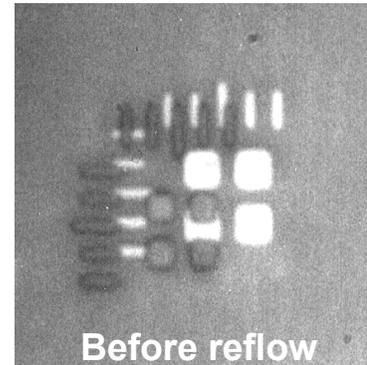
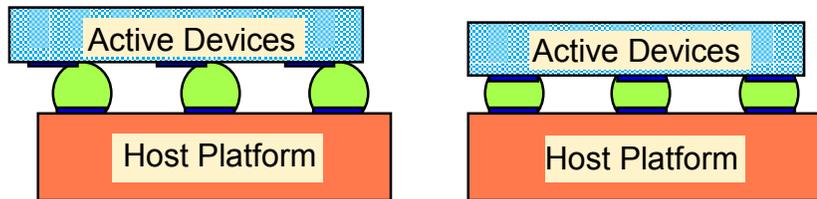


GaAs  
(Pd,Zn)  
Si

# High Resolution Self-Aligned Flip-Chip Bonding Process



High Resolution Passive Self-Alignment Upon Reflow

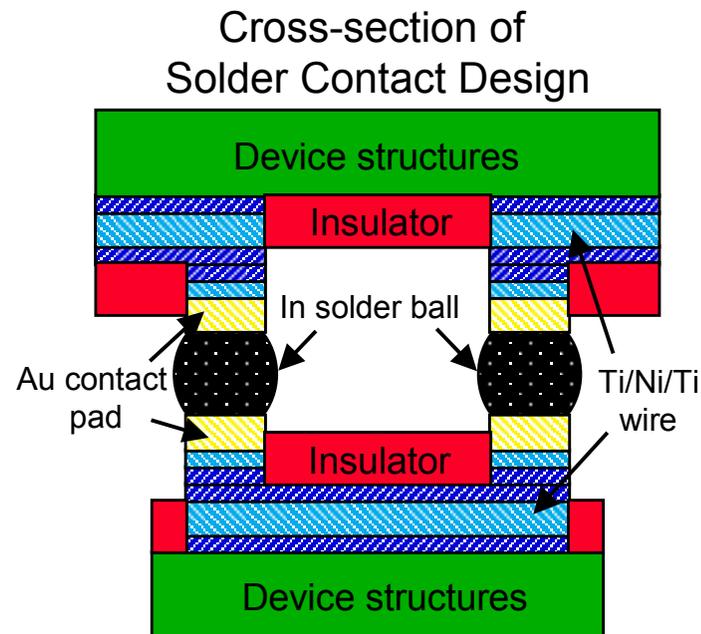
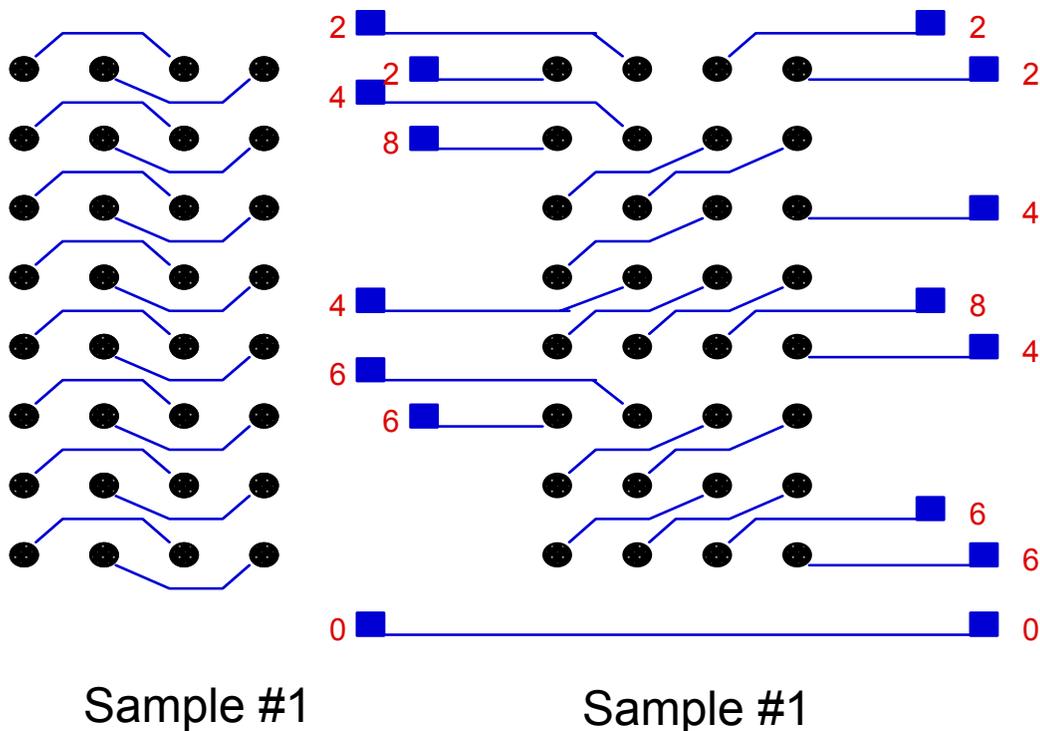


- ❖ Solder materials: 96.5 wt. % Sn + 3.5 wt. % Ag
- ❖ Reflow at 200°C to form solder balls
- ❖ Passive self-alignment resolution  $\leq 0.25 \mu\text{m}$

# Flip-chip Bump Bonding Technology Using Indium Solder Balls

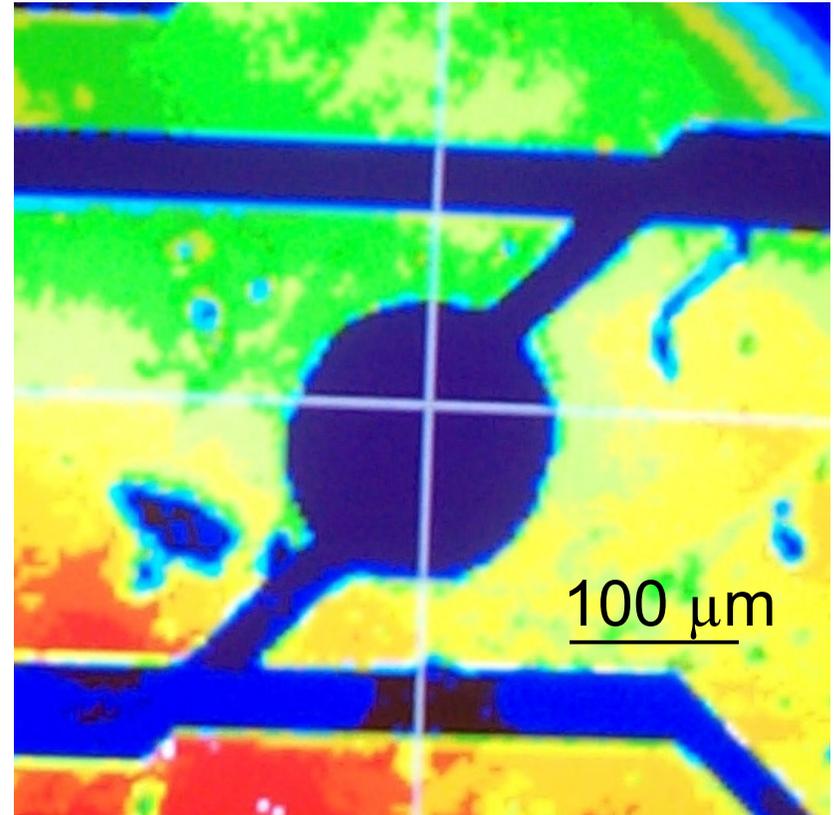
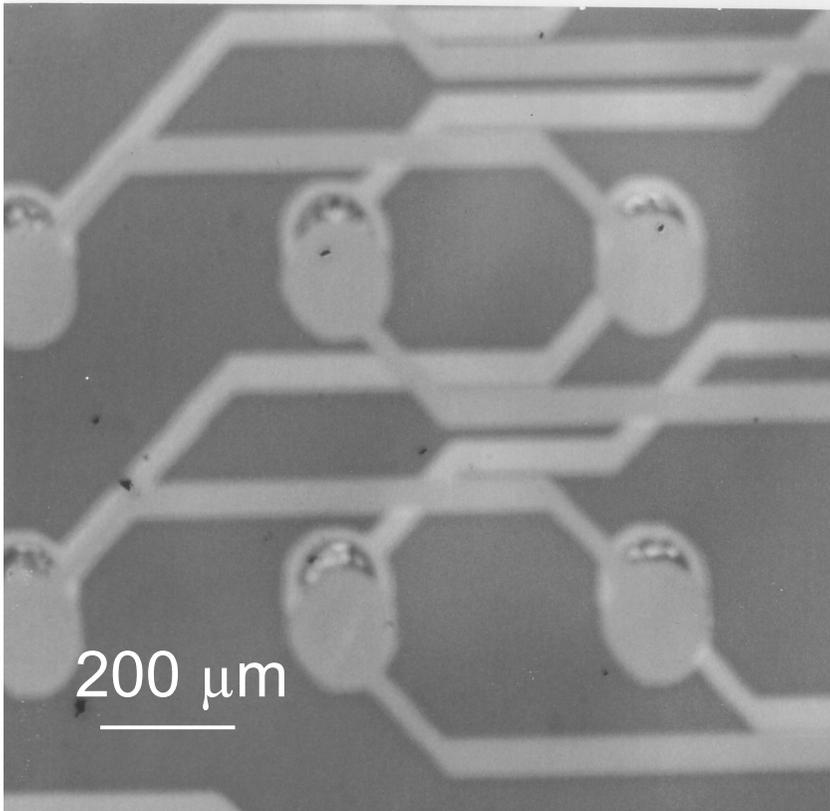


Bonding samples #1 and #2 through arrays of 4x8 solder balls



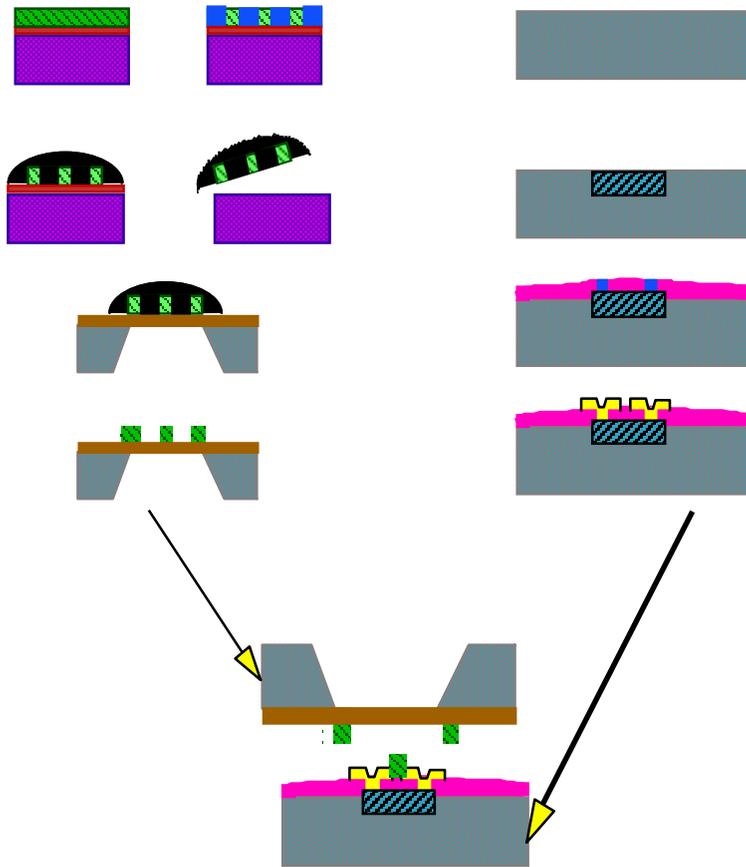
- ❖ Indium solder balls (size of 150 or 50  $\mu\text{m}$ ) are patterned on glass slides.
- ❖ Demonstration of bonding capability in a 4x8 array of indium solder balls.
- ❖ Good conductance through is measured 2, 4, 6, and 8 bonds in series.

# Optical and Infrared Micrographs of Flip-chip Indium Solder Bump Bonded Structures



- Demonstration of flip-chip bump bonding of two 4x8 In solder bump arrays delineated on two separated glass slides.
- Reflow temperatures at 350 ~ 400 °C with In bump sizes of 50 and 150 μm.

# Thin Film Integration Process for Heterogeneous Integration onto Silicon CMOS VLSI

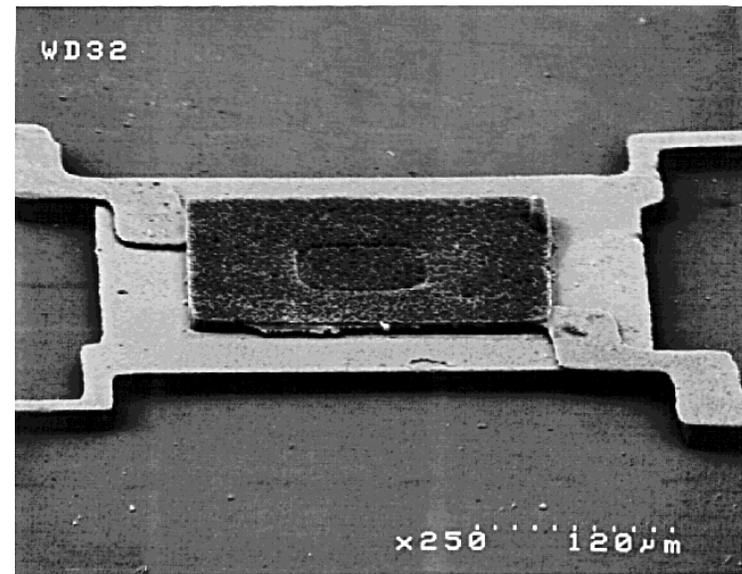
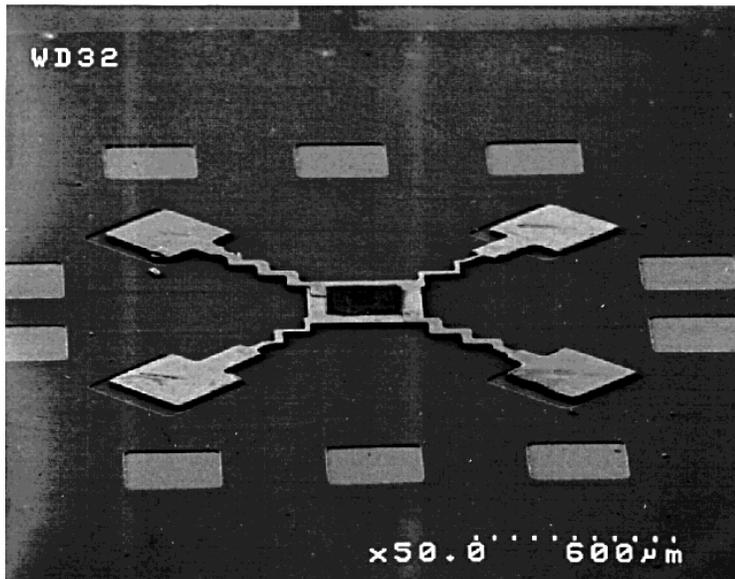


- Devices are patterned and metallized.
- The devices are mesa etched.
- Devices are protected from etchant with Apeizon W.
- The substrate is removed using wet etch solution.
- The devices are bonded to a transfer diaphragm.
- Apeizon W is removed with a solvent.
- Devices are aligned and bonded to host substrate using metal/metal bonding.

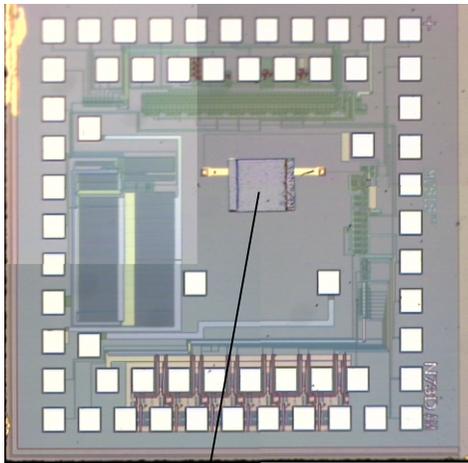
# Micro-Opto-Electro-Mechanical Integration



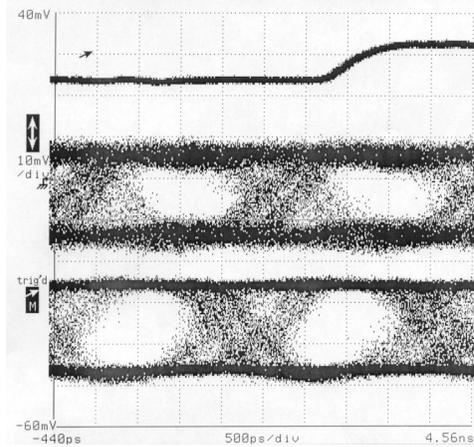
- ❖ Thin film P-I-N OE device bonded to micromachined movable (electrostatic actuator) platform on Si



# Large-Area InGaAs/InP I-MSM Integrated onto Si CMOS Receiver



InGaAs/InP I-MSM  
(250 x 250  $\mu\text{m}^2$ )



Eye diagram of differential  
Rx outputs at 414 Mbps



Eye diagram of comparator  
output at 414 Mbps

❖ *Demonstrated BER of:*

- $10^{-11}$  at 414 Mbps
- $0.1 \times 10^{-10}$  at 480 Mbps

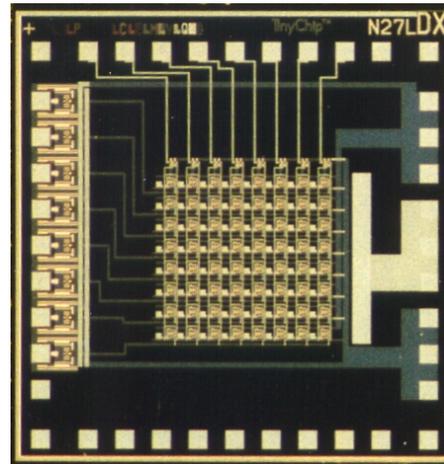
❖ ***A second proprietary system, same size detector, has BER of:***

- **$6.8 \times 10^{-10}$  at 1.0 Gbps**

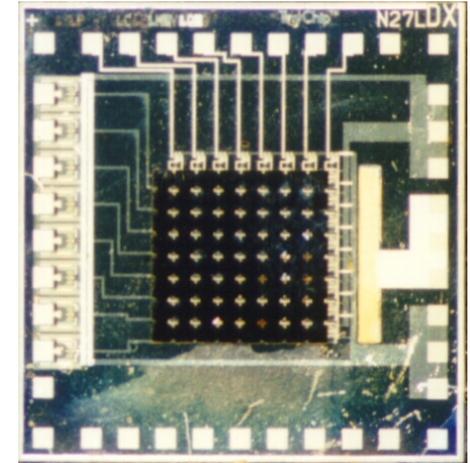
# Thin Film Heterogeneous Integration Onto Si CMOS VLSI



Thin film heterogeneous integration photo-micrographs for thin film GaAs/AlGaAs PIN detector array bonded to Si CMOS VLSI signal processing circuit

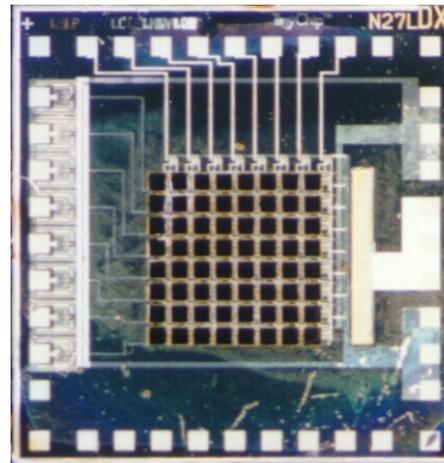


(a)

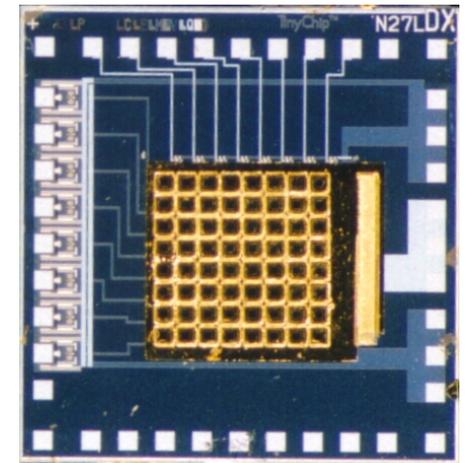


(b)

- (a) Si CMOS VLSI circuit
- (b) Thin film GaAs PiN detector linked array metal/metal bonded to Si CMOS circuit
- (c) Separation of array
- (d) Isolation and top metallization



(c)

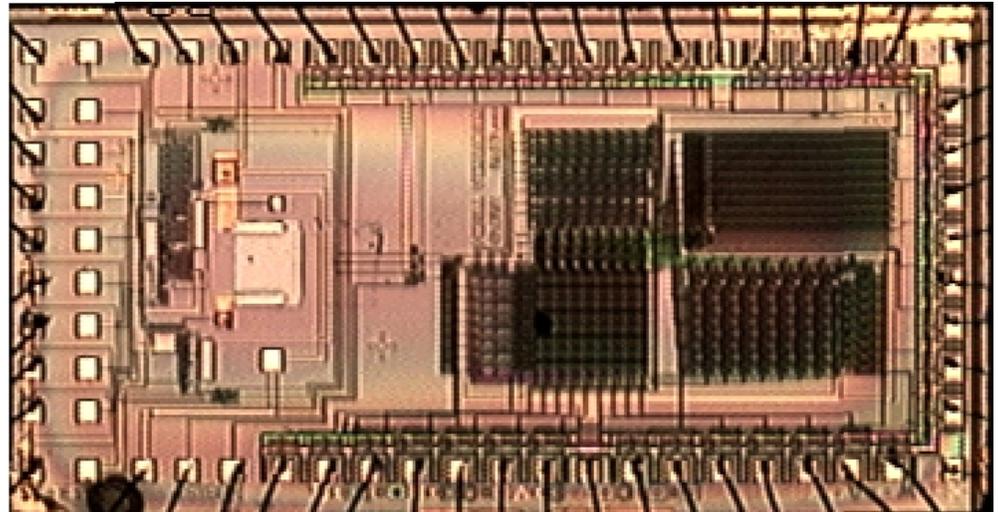


(d)

# Critical Issues for Heterogeneous Integration of Mixed Multi-Signal Systems



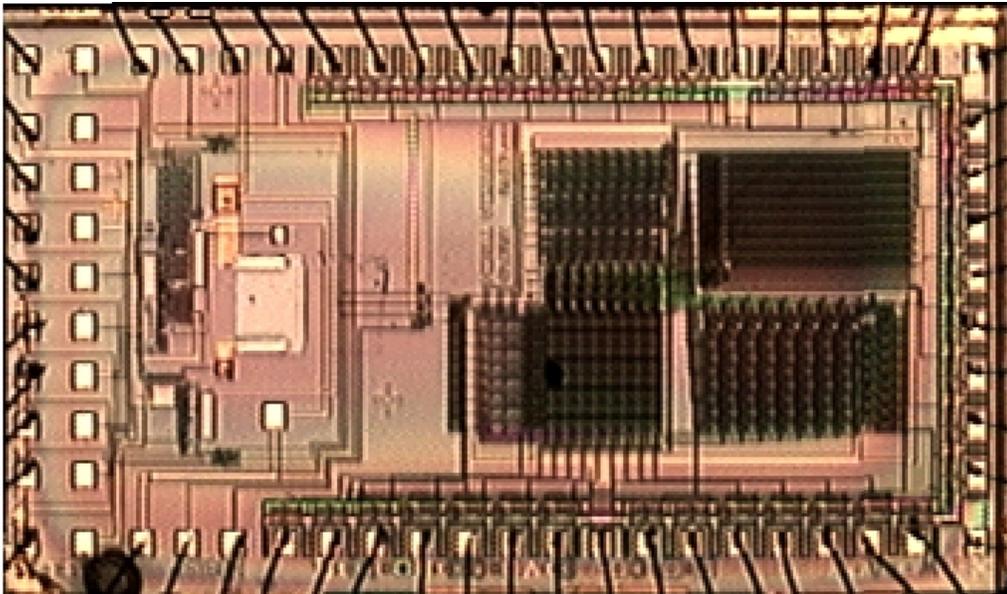
- ❖ Heterogeneous integration on Si CMOS VLSI seeks to attain high levels of signal processing with complex VLSI circuits
- ❖ High levels of Si CMOS VLSI digital signal processing create 100-500 mV of noise
- ❖ Integration of sensitive OE receivers with noisy digital Si CMOS VLSI into Mixed Multi-Signal (OE, digital, analog, and potentially, RF signals) create serious noise problems
- ❖ Thus, co-design of circuits and heterogeneous integration are essential to assure that mixed multi-signal systems will operate



# Single Chip Optically Interconnected Microprocessor Using Heterogeneous Integration onto Si CMOS VLSI

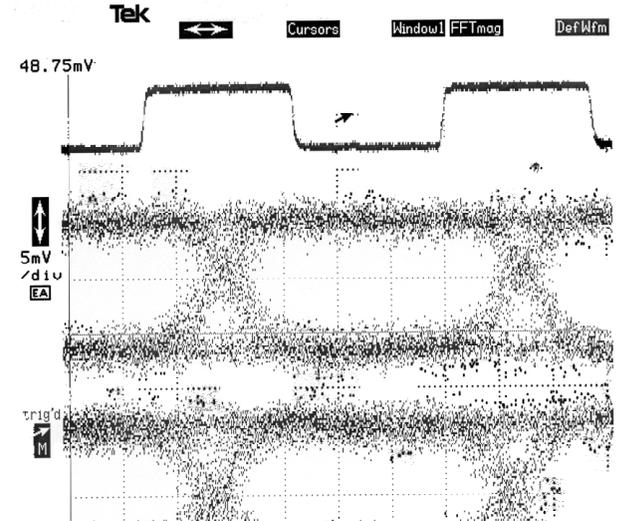


- ❖ Thin film InGaAs I-MSM detector bonded to Si CMOS analog differential receiver
- ❖ Digital Si CMOS VLSI "PICA" SIMD image processor on same chip
- ❖ Mixed signal challenge



## 100 Mbps operation

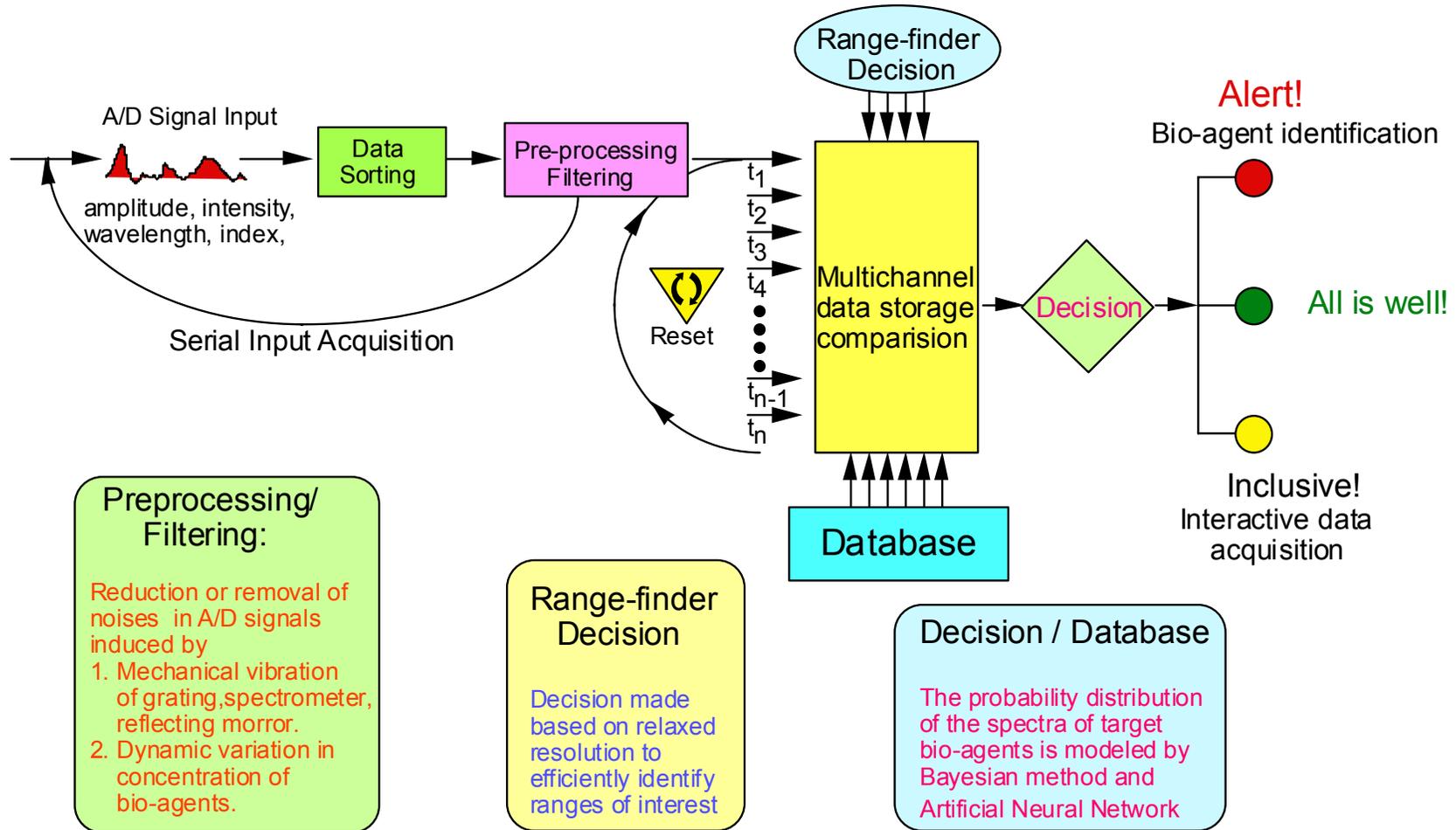
11403A DIGITIZING OSCILLOSCOPE {exp:3.6,dig:3.0,dsy:3.13}  
 date: 5-AUG-99 time: 15:41:15 Instrument ID# B011601



8.3  $\mu$ W O input,  $10^{-9}$  BER

-1.25mV	-10.56ns	2ns/div	9.44ns
			Main Size
			2ns/div
			Main Pos
			-10.8ns
Persist/	Mask	Color Grad	Remove/CirPan/
Histograms	Testing	Scale	Wfm 2 Zoom
Variable			L2 Off
Continuous			Main

# Data Acquisition / Information Fusion



# Multi-level Decision Making



Goal: To fuse together chronological information and decisions derived from various sources, mechanisms or previous decisions in order to make the final decision with an improved accuracy

