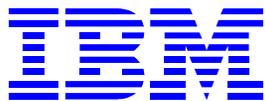




# C2OI Kickoff Meeting 6/18/2003

***Michael Tan***  
***Agilent Laboratories***

*June 23, 2003*  
*Westfields Marriott*  
*Chantilly, Virginia.*



**Agilent Technologies**



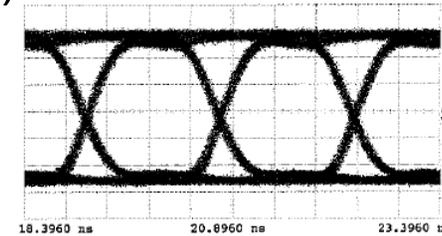
# Outline

- Agilent capabilities and past results
- Project Goals
  - Explore limits of VCSELs
  - High density PD arrays
  - Explore microresonator based EA modulators
- Milestones



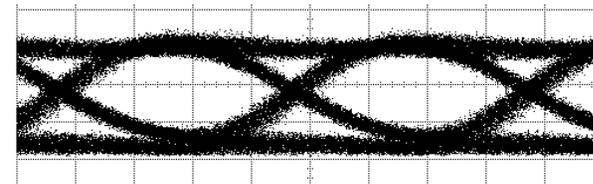
# Background: VCSELs at Agilent

POLO : 622Mb/s 980nm VCSELs (discrete)



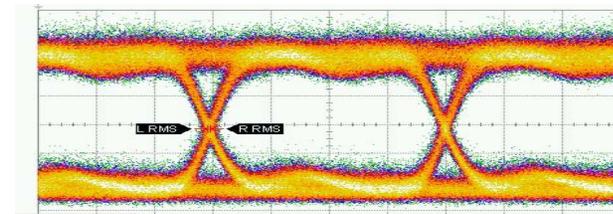
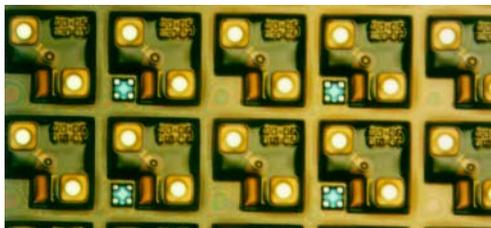
500 psec/div

PONI : 2.5Gb/s 850nm VCSEL arrays



100 psec/div

MAUI: 990, 1020, 1050, 1080 nm VCSEL @ 2.5Gb/s

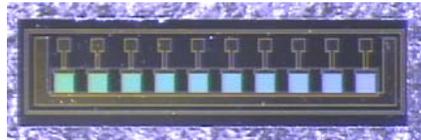


100 psec/div

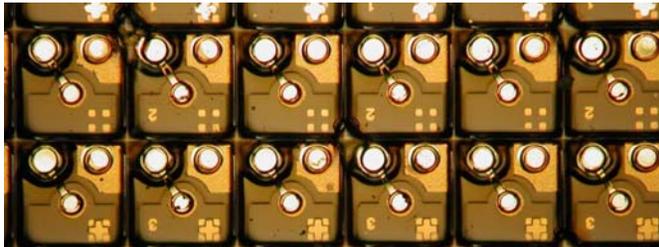
# Background: PD at Agilent

POLO : 622Mb/s InGaAs Photodetectors

PONI : 2.5Gb/s MSM & GaAs PIN arrays

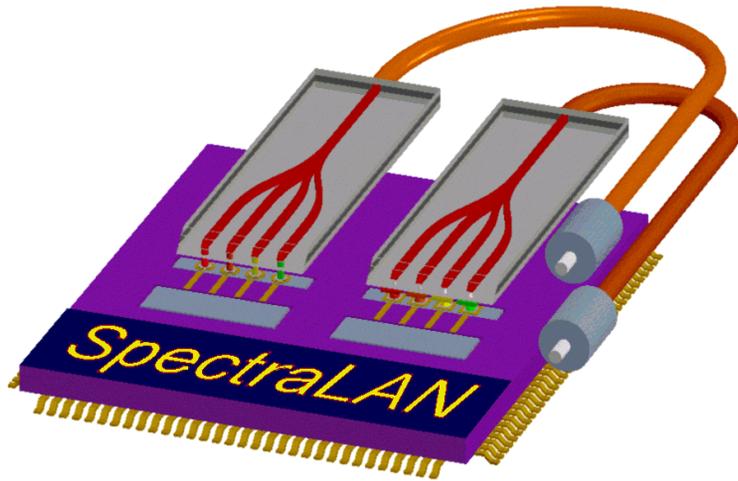


MAUI: 2.5Gb/s InGaAs PIN Photodetectors



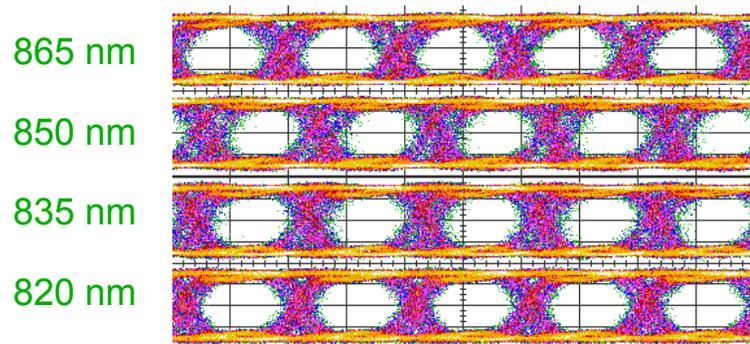
# Background: CWDM at Agilent

SpectraLAN-SX project 1995 – 1998



- Short wavelength VCSEL sources
- GaAs PIN detectors
- Si Bipolar Parallel Tx and Rx ICs
- Polymer waveguide optical mux and demux

4 x 2.5-Gb/s after 100 m 62.5- $\mu$ m MMF



**First 10-Gb/s CWDM solution demonstrated in 1998.**

*Leveraged Technology from DARPA-funded POLO Program*

# Agilent Capabilities

# Facilities



## **Aixtron 2000 Planetary Reactor**

Capacity:

5x3" wafers, 7x2" wafers

Materials Capabilities:

AlGa(In)As, AlGaInP, GaInAsP



## **Thomas Swan MOCVD Reactor**

Capacity:

3x2" wafers

Materials Capabilities:

AlGa(In)As, AlGaInP, GaInAsP

# Facilities



## Device Fabrication

- Evaporators
- PECVD
- ICP Etcher
- Photolithography
- E-beam



## Optical Link Testing

- High-Speed Analysis
- Over-Temperature
- Device Characterization



## Packaging/Assembly Area

- Wedge & Ball Bonding
- Flip-Chip Attach
- Passive/Active Aligners

# TERABUS: Optoelectronics

## Optoelectronics Agilent will develop under TERABUS

- Optimized VCSELs and photodiodes for high speed (>15Gb/s) and low power operation
- Flip-chip high density 2D VCSEL and photodiode arrays
- Low voltage  $\mu$ resonator electroabsorption modulator

# VCSEL Goals

Clean  $>15\text{Gb/s}$  Eyes (rise and fall times  $\sim 25\text{ps}$ )

High Temperature Operation (at least  $85^\circ\text{C}$ )

Low current density (for reliability)

High density, flip-chip 2D arrays

High-Speed Test Methodologies

Prototypes

# Photodiode Goals

Bandwidth > 20 GHz

Low  $V_{op}$ ,  $C_{tot}$ ,  $R_s$

Flip-chip, high density 2D arrays

Manufacturable Process

Prototypes

# Plan of Attack

*Rise and Fall Time → 25ps*

## ***Big Knobs:***

Increase Laser Relaxation Frequency

Reduce Device Capacitance

# Relaxation Frequency

$$f_r^2 = \frac{v_g a}{V_m q} \cdot \eta_i (I - I_{th}) = \left[ \frac{v_g}{q L_{cav}} \right] \cdot \eta_i \cdot a \cdot (J - J_{th})$$

Maximize differential gain,  $a (= dg/dN)$

→ Strained InGaAs MQW

→ Increase No of quantum wells

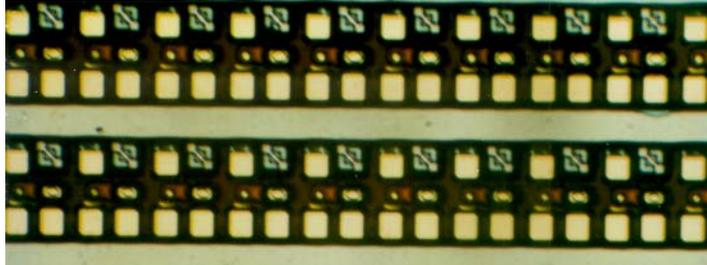
Increase  $J - J_{th}$

→ Failure rate  $\sim J^3$

Reduce Mode Volume

→ reduce  $L_{cav}$

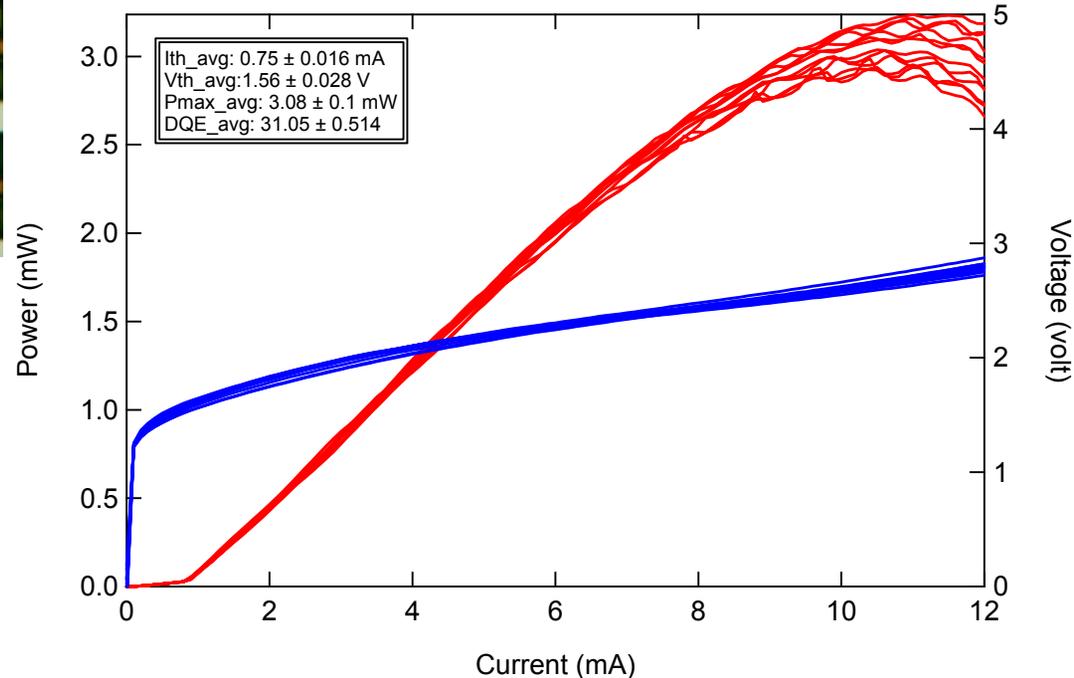
# 10 Gb/s 990nm BE VCSEL Array



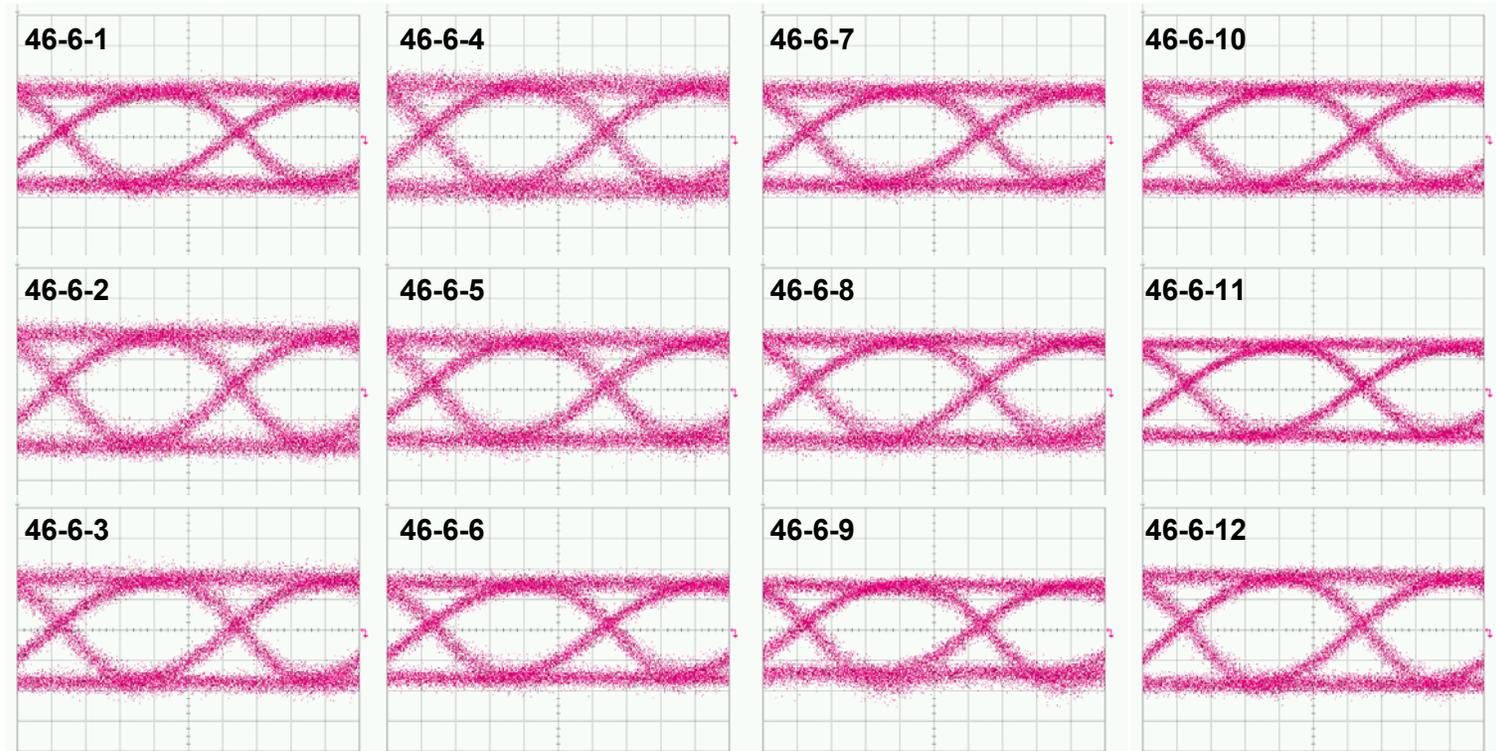
## 990nm oxide confined VCSEL

- $I_{th} = 0.75$  mA
- $V_{th} = 1.56$  V
- $DQE = 31\%$
- $P_{max} = 3$  mW

LIV Characteristics of 1x12 array

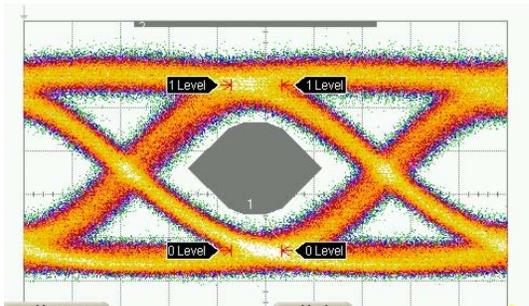


# 10 Gb/s 1x12 array



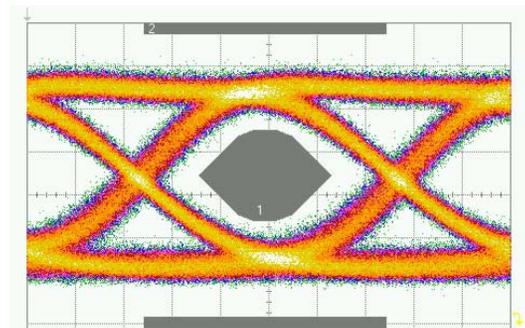
# 10Gb/s Performance vs Temperature

25°C



- $I_{bias} = 2\text{mA}$
- ER = 5.97 dB

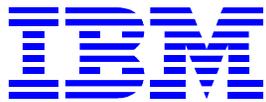
83°C



- $I_{bias} = 2.5\text{mA}$
- ER = 6.77 dB



## *High Density Photodiode Arrays*



**Agilent Technologies**



# Photodiodes for Chip to Chip computer Interconnects

**Objective:** Develop photodiode arrays suitable for high density chip to chip interconnects

Existing photodiodes are based on singlet designs

- Current processes are not high yielding for arrays
- Need shielding for light and cross talk control
- As speeds go up responsivity goes down or migrate to edge detectors which are hard to package

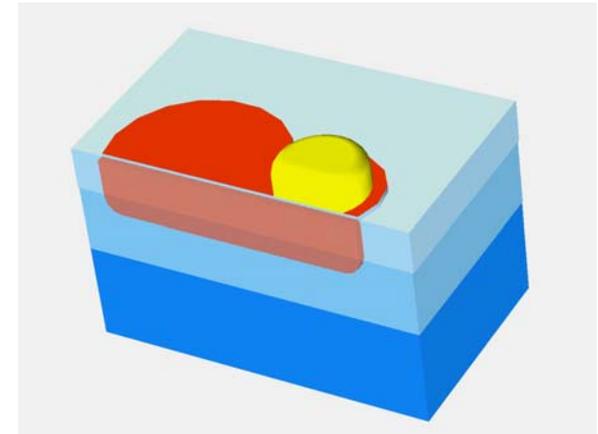
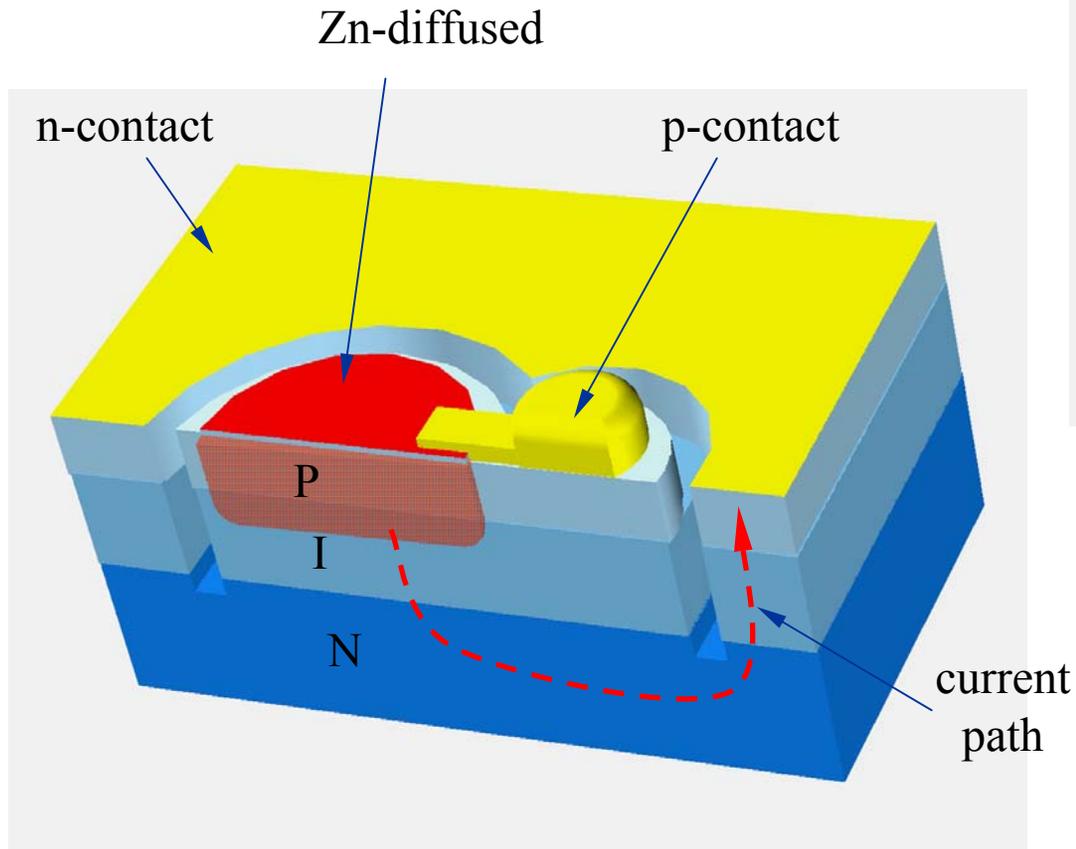
As speeds increase control of physical parameters becomes more important

- capacitance control, mesa diameter

Proposing new structure

- Grown in junction for control
- Bandgap engineering for greater response in surface normal device
- Improve Zn diffusion as backup

# PIN Device



Zn-diffused PIN  
(six masking steps)



# Photodiodes for Chip to Chip computer Interconnects

## Three Main areas for PD array improvements

### Improvements to individual photodiode performance

- Band gap engineering to eliminate carrier trapping at the respective hetero-interfaces and maximizing photo carrier transit speed.
- Low RC designs for bond pads and metal contacts and connections

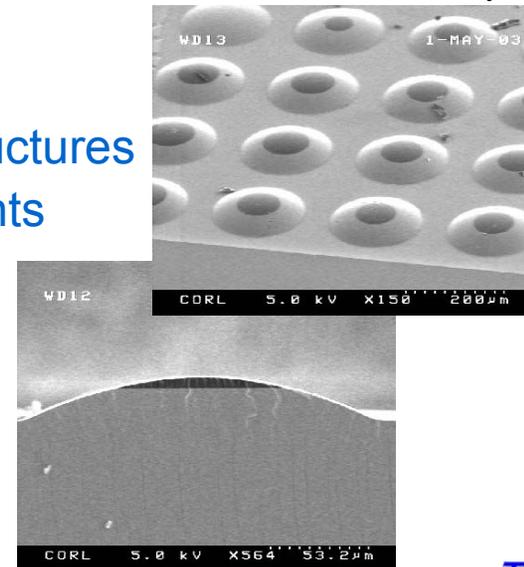
### Robust photodiode process

- Metal shielding to prevent optical and electrical cross talk
- In process controls to improve the yield of arrayed devices

### Ease of Integration into design environment

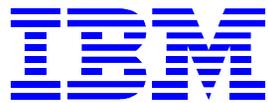
- Provide lumped circuit element models
- Fiducials for ease of assembly in flip-chip structures
- Backside lens for relaxing assembly constraints

Backside Lens Array





## *Microresonators*



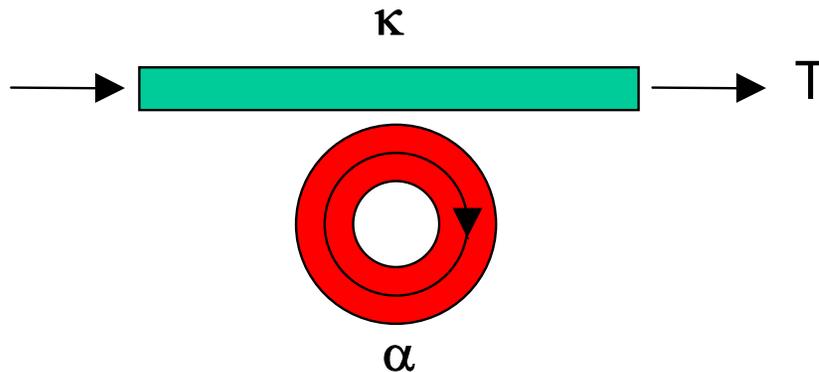
**Agilent Technologies**



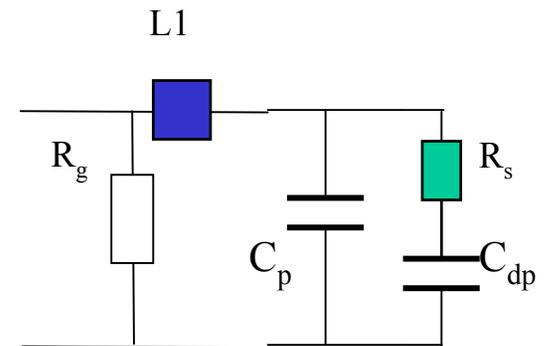
# Microresonators

## Microresonators EA modulators

- Lower drive voltage modulators
- Trade off Q with voltage drive

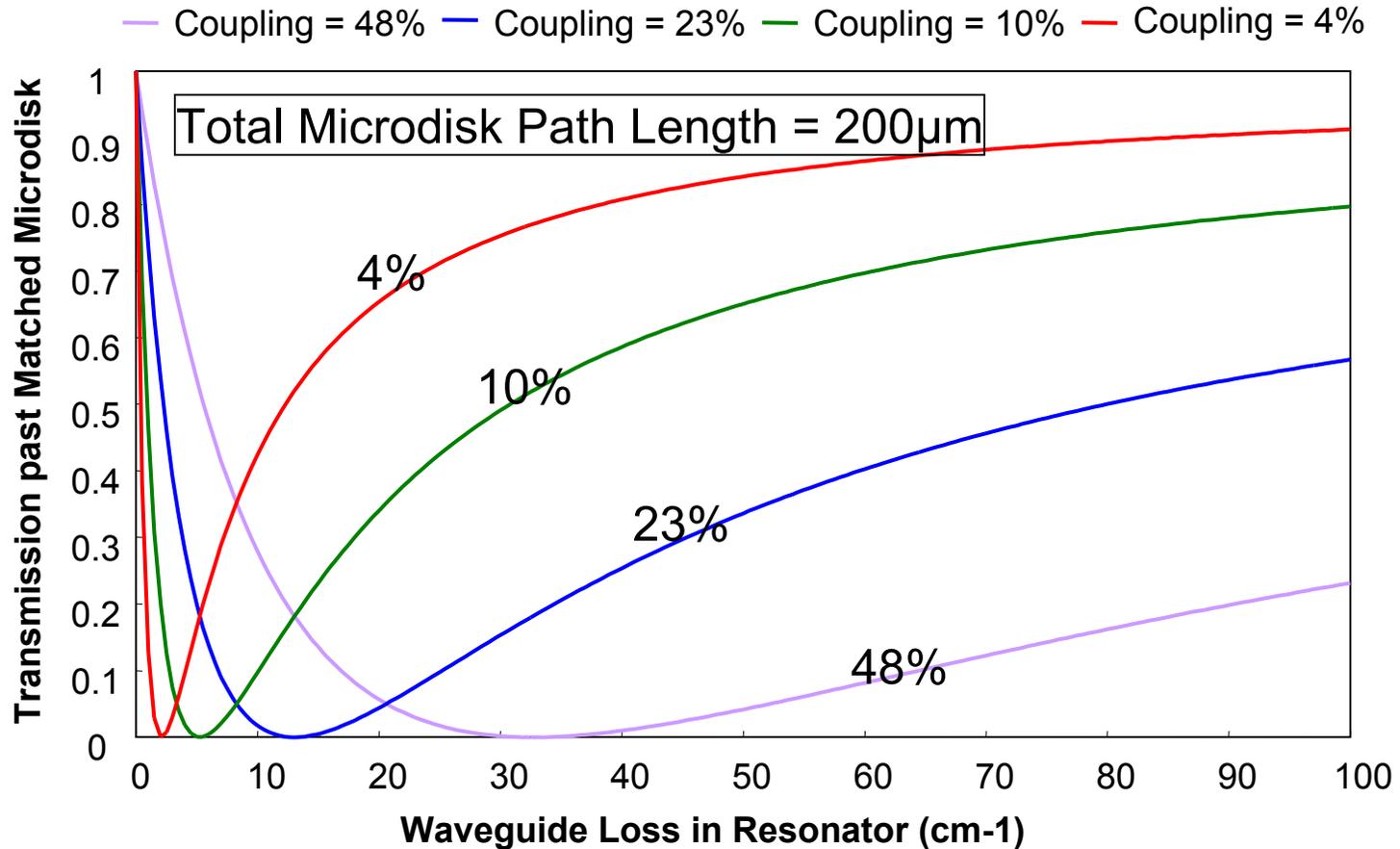


Modulator Equiv. Ckt

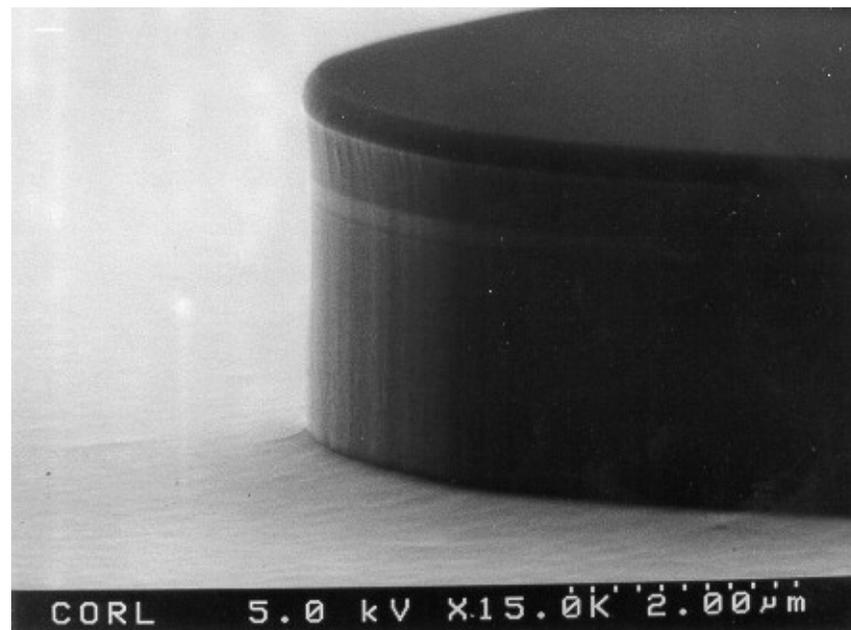
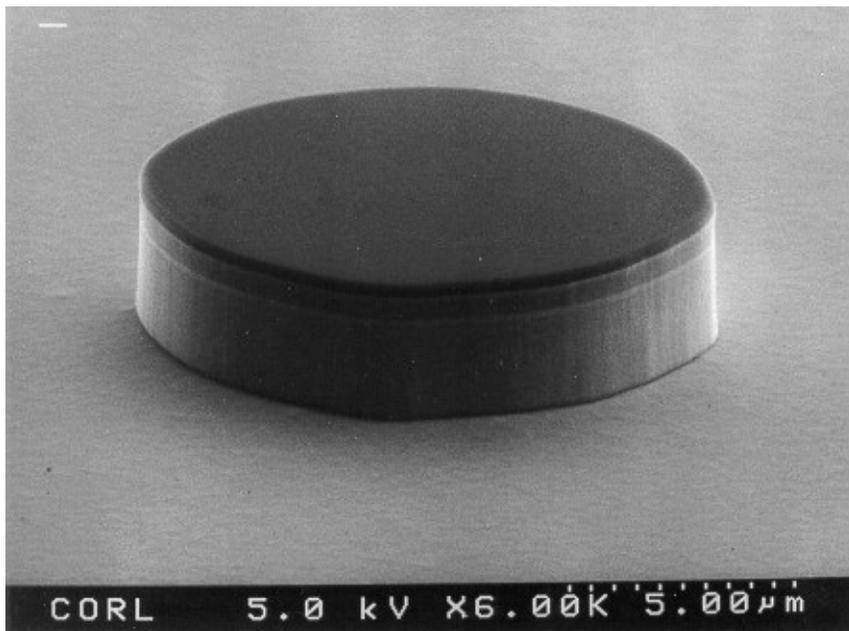


# Transmission vs Coupling

## Transmission vs Percent Coupling to Resonator



# Dry Etch for Micro Disk



# Terabus (Optoelectronics): Milestones

**Month 3: VCSEL and Photodiode specifications**

**Month 6: 1x12 UBM 10Gb/s VCSEL and (mechanical) PD arrays**

**Month 9: 4x12 UBM 10Gb/s VCSEL and (mechanical) PD arrays**

**Month 12: 4x12 UBM 10Gb/s PD arrays; modeling of  $\mu$ disk EA modulators**

**Month 15: 15Gb/s VCSEL and PD; waveguide/  $\mu$ disk process development**

**Month 18: 4x12 UBM 15Gb/s VCSEL and PD arrays; Optimize EA design**

**Month 21: Investigate VCSEL for > 15Gb/s. Finalize  $\mu$ disk EA modulator design**

**Month 24: Demonstrate passive waveguide/ $\mu$ disk integration.**

**Month 27: 3<sup>rd</sup> generation VCSEL and PD arrays; 1<sup>st</sup> (DC)  $\mu$ disk EA modulator**

**Month 30: Fabricate high speed  $\mu$ disk EA modulator**

**Month 33: Demonstrate 10Gb/s  $\mu$ disk EA modulator; 20Gb/s PD arrays; 4<sup>th</sup> gen VCSELs**

**Month 36: Demonstrate 40Gb/s  $\mu$ disk EA modulator; 40Gb/s PD arrays.**

