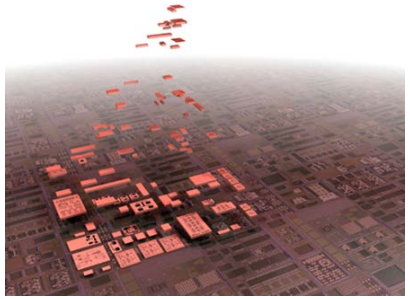
CHIPS Update

Access to DARPA CRAFT Multi-Project Wafer Runs
14nm/16nm FINFET process



November 16, 2016

Update

- CHIPS performers may access DARPA CRAFT Program MPW runs in advanced CMOS (16nm TSMC FinFET Compact process).

- To help provide some clarity on the CHIPS BAA Part II section G (see below), this document provides:
  - Background on DARPA CRAFT program and multi-project wafer runs.
  - Step-by-step guide to initiating contact with MOSIS.
  - What to expect next.

G. Government Furnished Equipment/Property/Information

No IP is currently provided for CHIPS performers, however the Government will provide public notice if specific IP blocks become available. The government will provide access to wafer processing runs in advanced Silicon CMOS technology via the capabilities established in DARPA/MTO's CRAFT program. The details and associated costs, which should be included in any CHIPS proposal, can be obtained upon request at:
https://www.mosis.com/db/pubf/cact?page_type=doc_access_req

Background on CRAFT and MOSIS

- MOSIS is an integrated circuit multi-project wafer (MPW) fabrication service provider.
- MOSIS is acting as the intermediary for MPW runs for DARPA's CRAFT program.
  - MOSIS can provide cost, MPW schedule, PDK, etc.
  - CHIPS performer tapeout data for CRAFT MPWs will be delivered to MOSIS.
  - MOSIS will coordinate mask build / wafer fab with the foundry.
  - MOSIS will deliver completed tiles to performers.

- BAA provides a link on Page 16 (Part II, Section I.G) to MOSIS to obtain CRAFT program details.
  - The address is repeated here for convenience
    - URL: https://www.mosis.com/db/pubf/cact?page_type=doc_access_req
  - CRAFT BAA may be accessed at this address
    - URL: https://www.fbo.gov/spg/ODA/DARPA/CMO/DARPA-BAA-15-55/listing.html

Please reference latest CHIPS and CRAFT BAAs and associated FAQs for the most up to date information, since this document may not be subject to revision control

CRAFT Program MPW Highlights

- Planned runs in TSMC 16**FFC** process.

- MOSIS can provide:
  - TSMC 16FFC PDK
  - TSMC 16FFC Foundation IP
    - Standard cells, Memories, GPIO
  - MPW runs planned:
    - MPW1 already in fab
    - MPW2 GDS-in April ‘17
    - MPW3 GDS-in ~Jan ‘18
    - MPW4 GDS-in ~Jan ‘19

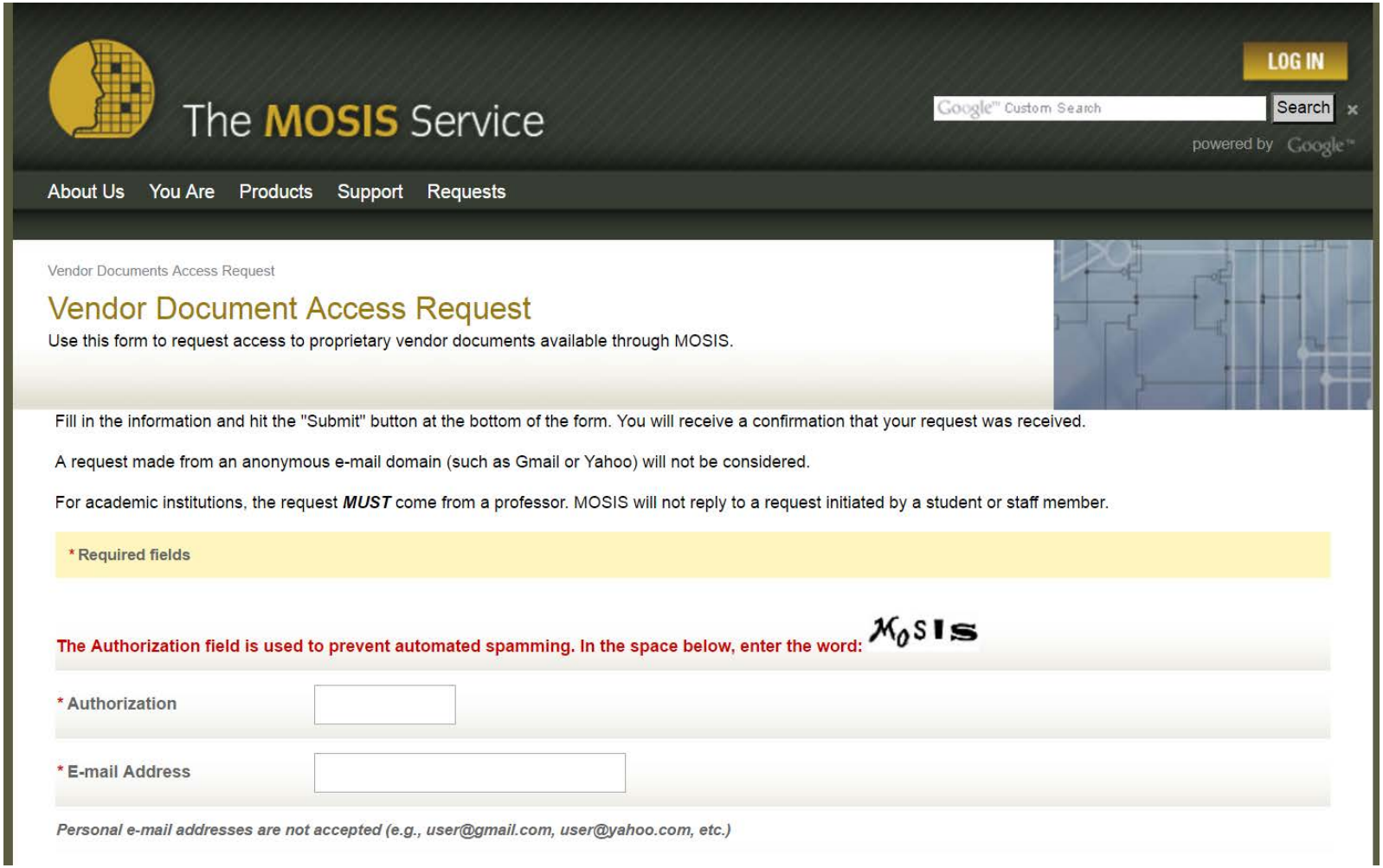
- CRAFT program tiles are sized 2.5mm x 2.5mm.

- Only supporting 9LM stack with 2 core Vt flavors and 1.8V IO.

Information provided for reference – please confirm latest data with MOSIS

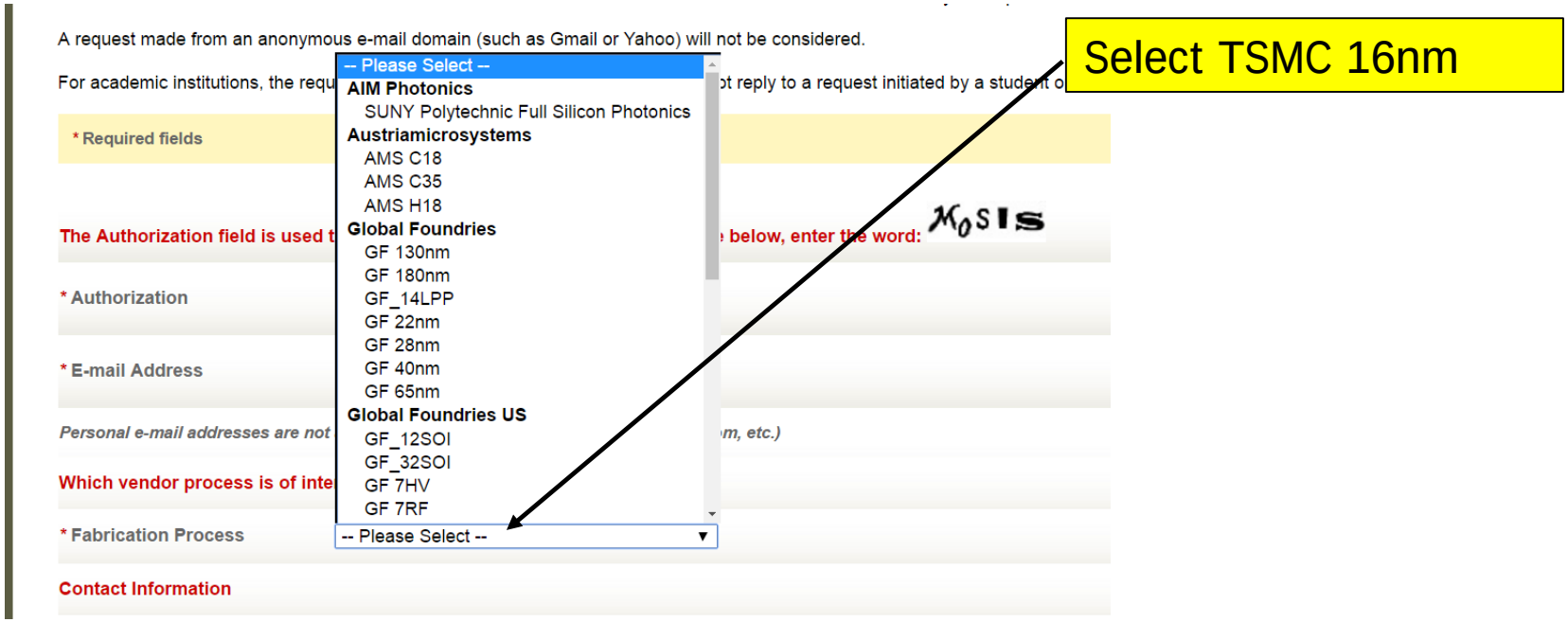
How to initiate access

- Following the link in the CHIPS BAA brings you to the MOSIS Vendor Document Access Request form.



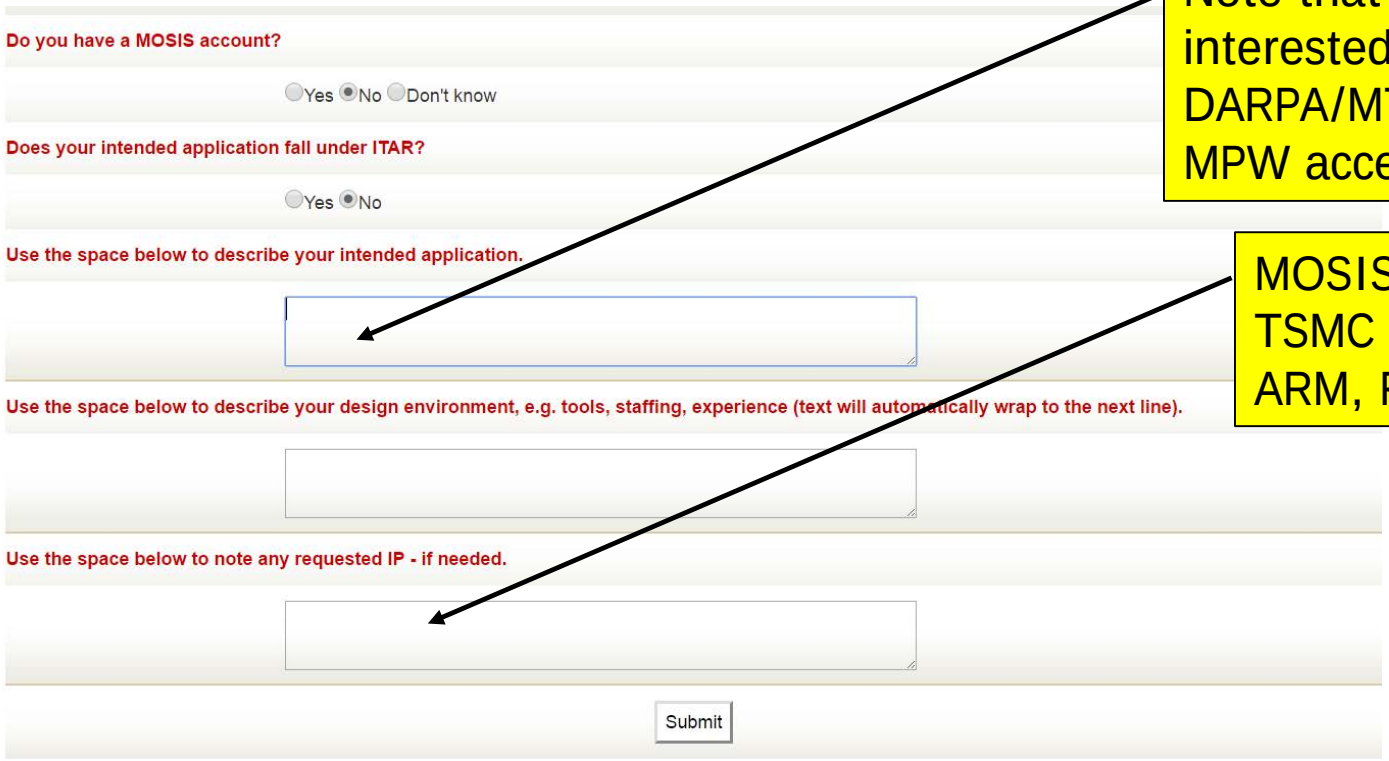
Filling in the form 1

- The first portion of the form is straightforward.
- For Fabrication Process input TSMC 16nm.



Filling in the form 2

- Fill in remainder of form.
- Note that TSMC is located in Taiwan. It is the performers responsibility to comply with all ITAR requirements.
- A MOSIS account is not required to complete the form, but **will** be required to receive PDK, IP, perform tapeout, etc.

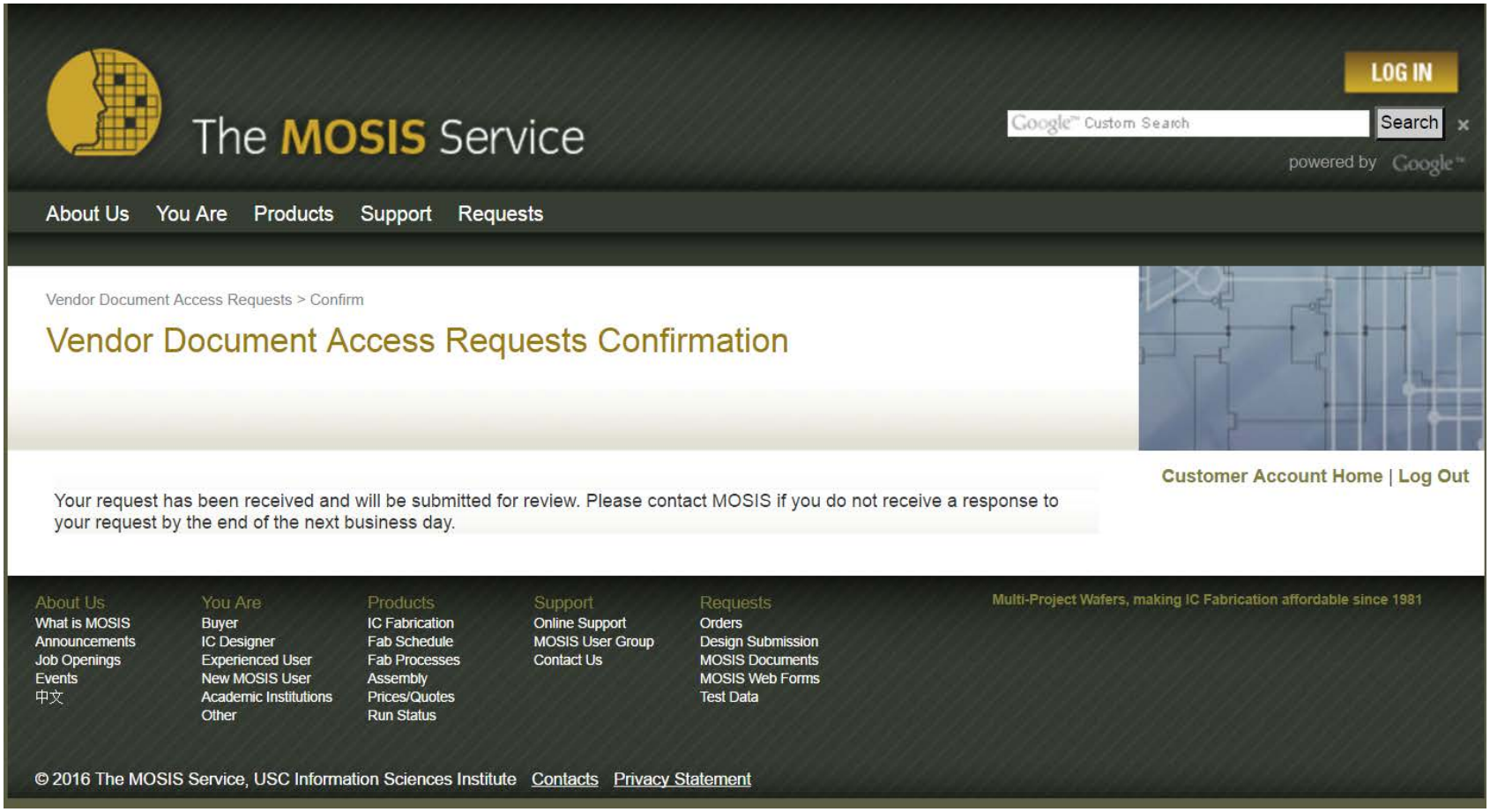


Note that performer interested in DARPA/MTO CRAFT MPW access

MOSIS only providing TSMC standard IP (no ARM, FPGA, etc).

After submission of form…

- Confirmation message should appear (below).
- MOSIS Rep should be in contact by the end of the next business day.



Process After Registration

- Completion of process triggers engagement with MOSIS.
- MOSIS will reply within 24-48 hours.
  - Should be able to provide tile cost, MPW schedule, etc. promptly.
- NDA and MOSIS account will be required to receive any technical data or PDK element.

Further Questions:

DARPA-BAA-16-62@darpa.mil