UPSIDE FAQ

Q: Does the constraint on non-CMOS mean no CMOS FETs, or no device implemented using CMOS fabrication processes?

A1: We do require that it not be CMOS or fabricated in a CMOS process, at least not without additional specialized processing steps. The constraint is meant to drive the exploration of alternative devices that process information using the unique physics of the device. Devices that are compatible with a CMOS fabrication process are encouraged to ease future integration with CMOS technology.

Q: Will devices performing computation via unconventional mechanisms (e.g. tunneling or electron injection) in standard CMOS fabrication processes be considered responsive to Task 3 (Emerging Nanoscale Devices) of the BAA?

A2: No, a CMOS device performing computation via an unconventional mechanism would not, by itself, qualify as a valid response for Task 3. For the definition of Emerging Devices (ED) in the BAA, we require that it not be a CMOS device. The intent of the UPSIDE ED focus is to develop devices that are not on the mainstream ITRS roadmap. Examples of acceptable unconventional devices include memristors or spin torque oscillators. Furthermore, UPSIDE program goals, as stated in the BAA, are three orders of magnitude in increased performance and four orders of magnitude reduction in power consumption for the ED. If in fact a CMOS device used unconventionally could approach these goals, there is room to include it either in Task 2, which asks for an analog CMOS implementation or as an additional supplementary device approach.

Q: Does the MS CMOS implementation in Task 2 need to simulate or mimic the behavior of the emerging device IM in Task 3?

A3: The MS CMOS implementation is not necessarily a simulation of the ED IM. Both are implementations of the IM developed in Task 1, but the details in how the IM model is mapped to each set of hardware will most likely be different due to the specifics of the hardware components.

Q: Is UPSIDE asking for a neural inspired approach?

A4: UPSIDE is not a "neural" program, but neural inspired solutions are welcome. The program is "neural neutral" in that it will neither be biased for or against neural approaches. UPSIDE is primarily focused on meeting the stated performance metrics.

Q: Is Task 1C required, and if proposed to, should Task 1C be costed separately?

A: Task 1C is not required but if proposed should be costed separately.

Q: Are there any requirements or restrictions on the level of optimization in the proposed baseline IPP?

A: UPSIDE metric comparisons against the baseline IPP are intended only to demonstrate the improvements due to UPSIDE technology development. It is recognized that each proposer's Baseline IPP will be different, running on different hardware and with a range in initial performance, power consumption, and accuracy. Proposals will not be penalized for beginning with a highly optimized baseline IPP. Reviewers will consider both the proposed improvements against the baseline (delta) and absolute proposed goals against the current state of the art. Improvements that result from hardware optimization to the baseline that are not related to the UPSIDE approaches will not be factored into the overall assessment.

Q: How important to the UPSIDE proposals/solution is Deep Learning?

A: Deep Learning was mentioned in the BAA solely as an example of an unconventional approach. There will be no bias for or against proposals that utilize deep learning.

Q: Are proposers required to address all 3 tasks?

A: Yes. Proposers can leverage previous accomplishments to address a task but all 3 tasks must be performed and the deliverables satisfied. Furthermore, any additional work that does not support the 3 tasks cannot be funded.

Q: Is the expected deliverable from Task 2 a standalone solution that implements the IPP completely?

A: The final deliverable for Task 2 is a testbed that is able to execute the entire IPP, consistent with the Gold Version simulation from Task 1, using the MS CMOS chip based IM to cover as much of the IPP functionality as possible. The role of the test bed is to validate the function and provide measurements for the metrics. There are no requirements on the form factor or specifications of the test bed itself and it may consist of multiple parts operating together to form the whole IPP chain.

Q: Are there any fabrication requirements for the MS CMOS chip in Task 2?

A: No, there are no requirements related to the choice of fabrication node or ability to scale to other nodes. Proposers are responsible for arranging their own fabrication.

Q: Is comparison between the IPP's of Task 2 and Task 3 expected against the Gold IPP, the Baseline IPP, or both?

A: The intention behind requiring a comparison of the relative differences in performance in Tasks 2 and 3, against an ideal standard, is to demonstrate, with UPSIDE technology, the resulting orders of magnitude improvement in power and throughput while retaining accuracy. Comparison against the Gold IPP is required by the BAA. However, further comparison between any of the IPP's that demonstrates the effectiveness of the UPSIDE technology is welcome.

Q: Does UPSIDE expect the entire improvement in performance or power consumption to be from hardware innovation, or is it acceptable to account for improvements to the algorithms implemented?

A: UPSIDE expects throughput and power efficiency improvements related to both the chosen algorithms and the hardware in which the algorithms are represented to provide the overall improvements required by the BAA. A key UPSIDE objective is that the algorithm and hardware implementation is intrinsically linked in each task and is necessary to achieve the program goals.

Q: In the BAA there was no discussion of underlying pipeline security. Are solutions related to the security of the IPP encouraged?

A: UPSIDE is not focused on developing security for the underlying pipeline, however if security is already involved in the chosen pipeline it can be included in the total IPP.

Q: Are there any forms of imaging that would not be encouraged (Infrared, Broad spectrum, Radar, etc.) for the UPSIDE proposals?

A: Any imaging application of interest to the DoD is an acceptable response. Proposers should pick an application that most fully demonstrates the improvement gains from UPSIDE technology and that has the greatest possible impact for the DoD.

Q: Does the IM need to replace 100% of the pipeline computation and functionality?

A: It is not expected that the IM will be able to replace 100% of the computation in the IPP, but an attempt should be made to utilize the IM in as many places as possible within the IPP, which is necessary to achieve the maximum possible impact on the total performance and power consumption of the IPP.

Q: Are different IM configurations or complexities acceptable, so as to utilize the technology in more functions of the IPP?

A: The proposer is free to develop multiple variations and complexities of the fundamental IM for different functions within the IPP, since different IM configurations will most likely be necessary at different points in the image processing hierarchy, for recognition, for tracking capability or for back-end computation.

Q: When porting the GOLD simulation to a high performance platform, are there any required guidelines for the platform hardware or the resulting throughput increase?

A: There are no required guidelines for the platform hardware or specifics on the resulting throughput increase. The task of porting the GOLD IPP simulation to a high performance platform is intended to enable the processing of larger and higher definition video data more efficiently.