DAHI Foundry Technology BAA

Frequently Asked Questions

General Questions

Q – Is there a specific program start date that should be assumed for budgetary purposes in the full proposals?
A – No, there is no specific start date established at this time. However, we anticipate the DAHI Foundry Technology kickoff will take place in the late November or December timeframe.

Q – Are there specific budget levels or number of awards assigned to the different technical areas?
A – No, the number and amount of awards in each technical areas depends on the quality of proposals received and the available funds. However, note that we anticipate funding only 1 or 2 efforts in technical area II.

Q - Are multiple proposals from the same organization allowed?
A – Yes.

Q – Is the final substrate expected to be silicon? Will other substrate materials be considered?
A – As described in the BAA, "the goal of the DAHI Foundry Technology BAA is to develop advanced heterogeneous integration processes, allowing diverse material systems and device technologies to be tightly integrated on a common silicon substrate." For Technical Area I, "the proposed approaches under this Technical Area are <u>not</u> specifically required to be demonstrated on ≥200 mm wafers, but should have practical technical paths and plans to integrate the process module with or onto at least 200 mm diameter silicon wafers." On the other hand, "in Technical Area II, the proposer must develop the DAHI technology on ≥ 200 mm diameter silicon wafers and enable to provide the foundry service through multiproject wafer (MPW) runs during the DAHI program." Novel/engineered substrate materials with desirable properties, e.g. better thermal conductivity or mechanical robustness, may be considered as long as the overall BAA goals of 200mm silicon-based wafer format manufacturing as stated in the BAA for the applicable technical areas are achieved.

Q – Are there preferred devices/materials or fabrication approaches that are being sought in this BAA?
A – No, but proposers should carefully consider the guidance in the BAA regarding ability to enable revolutionary capabilities not possible without heterogeneous integration technology, ability to coexist with or incorporate other heterogeneous process modules, DoD relevance, etc.

Q – The BAA seems to emphasize semiconductor technologies; are novel non-semiconductor technologies also of interest?

A – Non-semiconductor technologies are of interest. In all cases, proposers should justify the value added of their chosen devices and materials (semiconductor or non-semiconductor) by describing their impact on heterogeneously integrated circuits with revolutionary performance and value for DoD applications.

Q – What types of heterogeneously integrated circuits are of greatest interest in this BAA?
A – Of greatest interest are circuits which demonstrate revolutionary performance and functionality which cannot otherwise be achieved without heterogeneous integration approaches. Additionally, relevance of the heterogeneously integrated demonstration circuits to DoD applications will be an important consideration.

Q – The BAA states that "process modules already available in silicon CMOS/BiCMOS technologies" are not considered to be novel heterogeneous integration technologies for the purposes of this BAA. What constitutes "already existing"?
A – If a process module (for instance, some MEMS process modules) is already available within the proposed silicon base technology or available within the broader silicon foundry industry, then that would not be considered to be a novel technology. However, it should be noted that the availability of such already existing process modules could be regarded as a valuable aspect of the base silicon technology if it is made available in a proposed DAHI foundry process.

On the other hand, it is possible that there may be certain device/material technologies that have been previously demonstrated on a silicon substrate (e.g. GaN on <111> silicon), but have not yet been integrated with advanced silicon CMOS, in which case this may be considered a new heterogeneous integration approach. Proposers should justify that integration of such a device/material with a silicon CMOS/BiCMOS base technology is revolutionary and not already available using existing process flows.

Q – This BAA emphasizes use of wafers of at least 200mm diameter. Can coring of wafers be used as a pathway for compatibility with 200mm wafers?
A – Coring would <u>not</u> meet the goals of Technical Area II, which specifies production of fabricated circuits on ≥200mm wafers. On the other hand, coring <u>would be</u> acceptable for Technical Area I, since it does not require fabrication on ≥200 mm wafers by the end of the program. However, Technical Area I proposals should describe "practical technical paths and plans to integrate the process module with or onto at least 200mm diameter silicon wafers." Note that the described transition to ≥200mm silicon wafers does not have to occur within the proposed Technical Area I effort.

Q – Can non-U.S. organizations participate in this BAA?
A – Yes, as long as applicable export and security regulations are complied with (see Sec. VI, B. 5. of BAA for additional information regarding export control).

Technical Area I

Q – The BAA states that Technical Area I proposers should describe "practical technical paths and plans to integrate the process module with or onto at least 200mm diameter

silicon wafers." Does this mean that proposers would need to show letters of support from potential collaborators to support this?
A – Proposers should provide clear and well-justified pathway to integrate their technology into a ≥200mm process flow during or after the conclusion of their proposed effort. Letters of support could be part of such a justification, but they are not strictly required.

Technical Area II

Q – How comprehensive does process design kit (PDK) data need to be for Technical Area II?
A – The provided PDK data files should be sufficient to enable outside parties to produce designs in industry-standard design environments and with capabilities such as verification, DRC checks, parasitic extraction, etc.

Q – For MPW runs, how much mask area should Technical Area II teams plan to reserve for use by MPW design participants?
A – This will depend on a number of factors, including the space required for proposed yield and reliability monitoring circuits, and will be determined during the course of the effort. The final decision on space allocation will be made between the government and the Technical Area II performer(s).

Q – How will MPW design participants be chosen?
A – These will be chosen by the government, and are expected to include at a minimum the Technical Area III design teams.

Technical Area III

Q – Should Technical Area III proposers budget funds in the cost proposal for area on the MPW runs?
A – No, the costs of DAHI foundry MPW run fabrication within the program will be covered by the Technical Area II performer budgets.

Q – At what level should Technical Area III teams focus their designs? For instance, should Technical Area III teams attempt to design complete systems?
A – The focus of Technical Area III is on the design of heterogeneously integrated circuits only – no higher-level system design is required. However, identifying relevant system applications and/or flowing down specifications for a proposed unique circuit could strengthen a proposal.

Q – Can Technical Area III effort include the improvement of integrated circuit thermal modeling using established CAD tools?
A – Yes. As stated in the BAA, Technical Area III activities can include "establishing DAHI design/simulation tool flows necessary to realize the full potential of heterogeneous microsystems integration."

Q – What will happen if Technical Area III teams propose using devices/materials that are not ultimately made available within the Technical Area II MPW offerings?
A – Since it is not known a priori what devices/materials will ultimately be made available in the foundry offering, it is recommended that Technical Area III teams demonstrate flexibility in their proposals to take advantage of a range of potential devices/materials in their proposed designs.

Technical Area Interactions

Q – How will interactions between Technical Areas I and II occur?
A – This BAA is seeking high risk, novel heterogeneous integration approaches in Technical Area I; it is envisioned that these may become transferrable to the Technical Area II foundry technology during the course of the DAHI Foundry Technology thrust, depending on how rapidly the Technical Area I technology or technologies can be successfully demonstrated . However, we do not expect this transfer to be a contract deliverable at the outset of the thrust. Note that the BAA states that "the proposals should reflect an approach that will yield a sustainable business practice either to establish a foundry offering for DoD users and contractors, or to transfer DAHI process modules to a DAHI foundry integrator of Technical Area II by transferring or licensing intellectual properties developed under the DAHI program or some other suitable arrangement."

During the program, Technical Area II performers will be strongly encouraged to collaborate with Technical Area I performers to identify opportunities to insert Technical Area I technologies into the Technical Area II process flow. As stated in the BAA, "At the end of the thrust, a DAHI technology integrator or foundry provider is expected to provide a scalable DAHI process integrating the initial three (or more) distinct technologies (including the silicon base technology), and also have the capability to support additional process modules."

Q – How will interactions between Technical Areas II and III occur?
A - Technical Area III proposers are encouraged to assess a variety of candidate materials and devices for developing heterogeneously integrated circuits with revolutionary performance and functionality for DoD-relevant applications. Early in the program thrust, Technical Area III teams will provide input to Technical Area II teams on their recommendations for the materials and devices that would enhance the capabilities of the DAHI foundry offering.

Technical Area II performers will supply process design kit (PDK) files to selected Technical Area III teams, as well as other government designated design groups, under appropriate NDA/design kit license agreements, in coordination with their multi-project wafer (MPW) offering schedule. Technical Area III teams will tape out design submissions for the MPW offerings, and Technical Area II teams will then supply fabricated circuits to Technical Area III teams in accordance with the expected Technical Area II deliverables.

Q – Due to uncertainties associated with the Technical Area interactions described above, is it possible that these interactions could be facilitated by contract modifications during the course of DAHI Foundry Technology thrust?
A – Yes, this is a possibility.