

DAHI Foundry Technology BAA Overview

Sanjay Raman, Program Manager
DARPA/Microsystems Technology Office

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 - Northrop Grumman Aerospace Systems (Redondo Beach, CA)
 - Raytheon (Andover, MA)
 - Aurion, Inc. (Goleta, CA)
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 - University of California, Berkeley (Berkeley, CA)
 - University of California, San Diego (La Jolla, CA)
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 - Office of Naval Research
 - US Navy Space and Naval Warfare Systems Command (SPAWAR) Systems Center Pacific (San Diego, CA)
 - National Institute of Standards and Technology (Boulder, CO)
- Subject Matter Experts:
 - Mr. Eliot Cohen
 - Dr. Richard Eden
 - Mr. Tim Kemerly
 - Dr. Dan Raddack (IDA)
- Dr. Mark Rosker (original program manager of COSMOS)
- Dr. Avi Bar-Cohen (DARPA/MTO PM)
- Dr. Scott Rodgers (DARPA/MTO PM)
- Dr. Thomas Lee (DARPA/MTO Office Director)

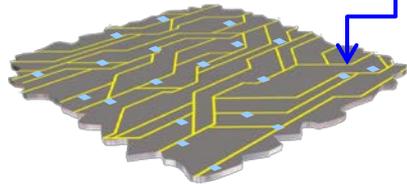
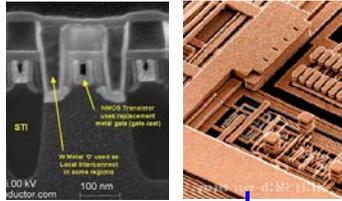


- DAHI Program Overview
 - DAHI Program Objectives
 - Program Challenges and Applications
 - Current DAHI Thrusts
 - Compound Semiconductor Materials on Silicon (COSMOS)
 - Electronic-Photonic Heterogeneous Integration (E-PHI)
- DAHI Foundry Technology BAA Overview

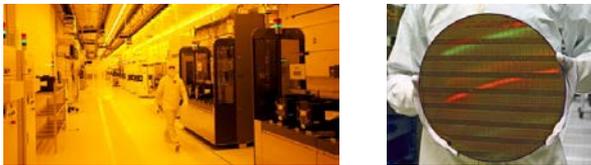


Diverse Accessible Heterogeneous Integration (DAHI): Objective

Today:
CMOS on Silicon substrate for complex information processing



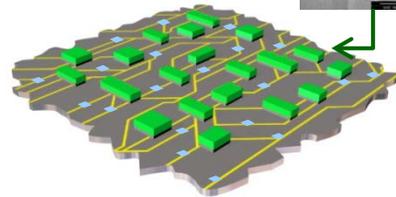
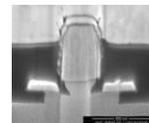
Fabrication in modern silicon fabs with full-size wafers.



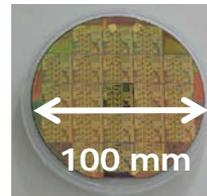
DARPA COSMOS

Demonstrated feasibility and value of transistor-level integration of indium phosphide (InP) devices with Si CMOS

High speed indium phosphide transistors



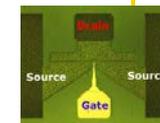
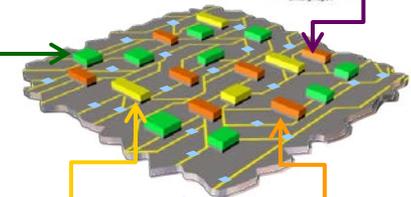
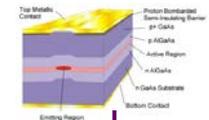
Fabrication in specialized small-scale/R&D fabs



DAHI

Heterogeneous Integration of diverse array of devices on common Si CMOS platform

High gain / efficiency III-V lasers/detectors (E-PHI)



High Johnson FOM gallium nitride transistors



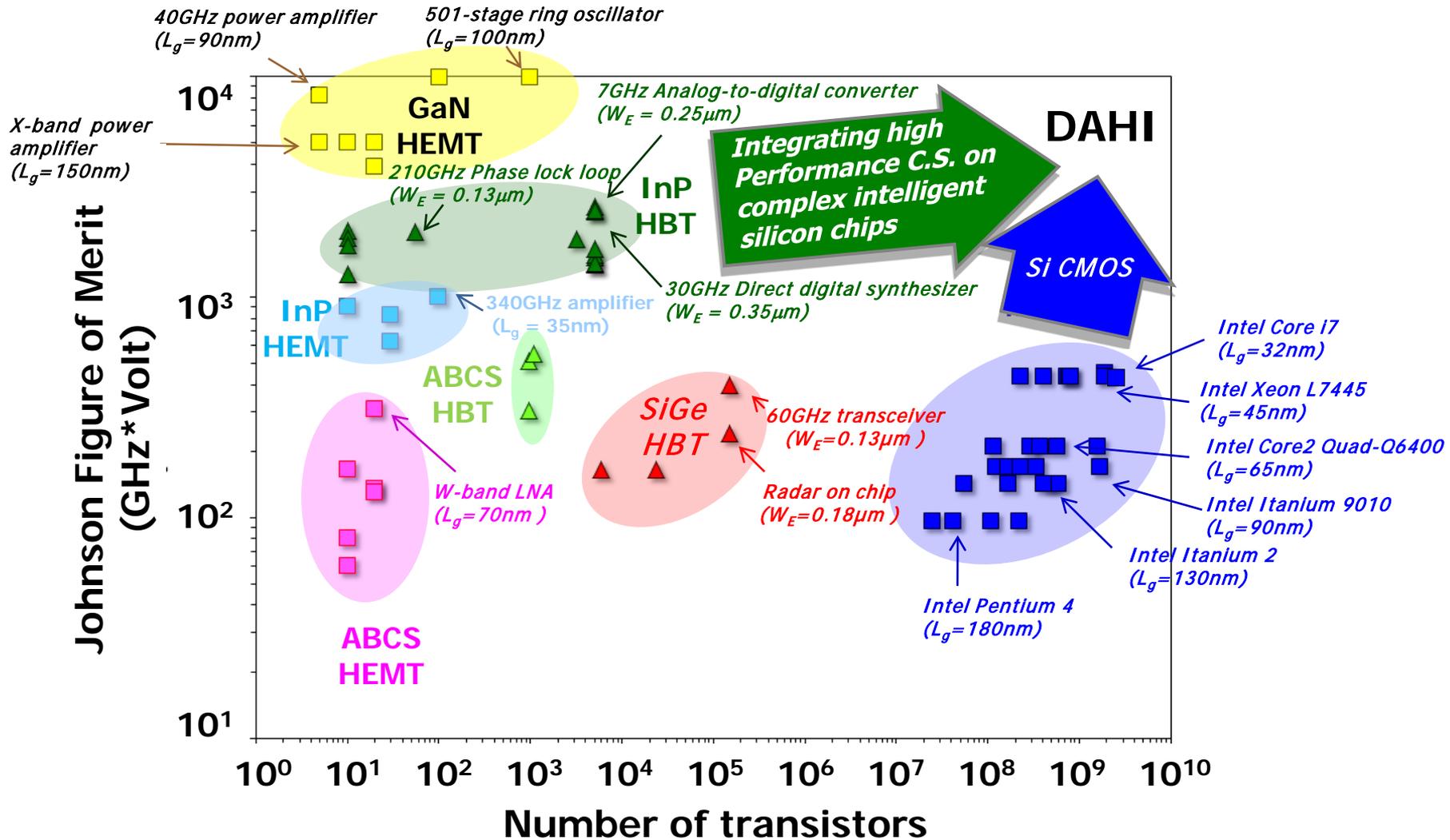
High Q, high linearity RF MEMS

The DAHI program seeks to: Enable a manufacturable, accessible foundry technology for the monolithic heterogeneous co-integration of:

- diverse devices (electronic, photonic, microelectromechanical [MEMS]...) – “best junction for the function”
- complex silicon (Si) complementary metal-oxide-semiconductor (CMOS)-enabled architectures
- a common silicon substrate platform



COSMOS motivation: Johnson figure of merit versus level of integration by device class

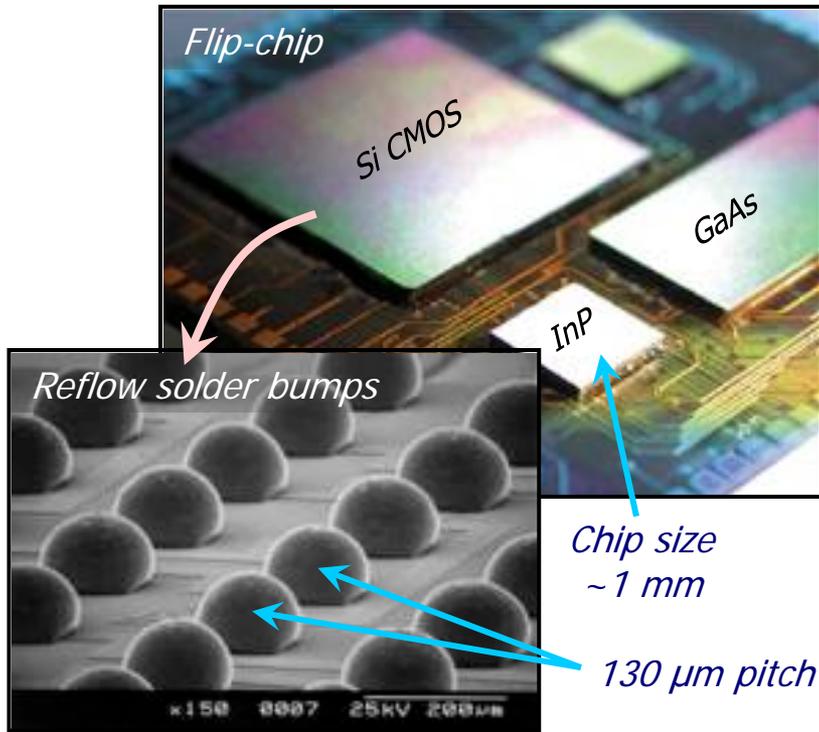


Terminology:

InP = indium phosphide, GaN = gallium nitride, SiGe = silicon germanium, ABCS = antimonide-based compound semiconductor
HBT = heterojunction bipolar transistor, HEMT = high electron mobility transistor, L_g = gate length, W_E = emitter width



Intimate Heterogeneous Integration: *pushing interconnect bandwidth limits...*

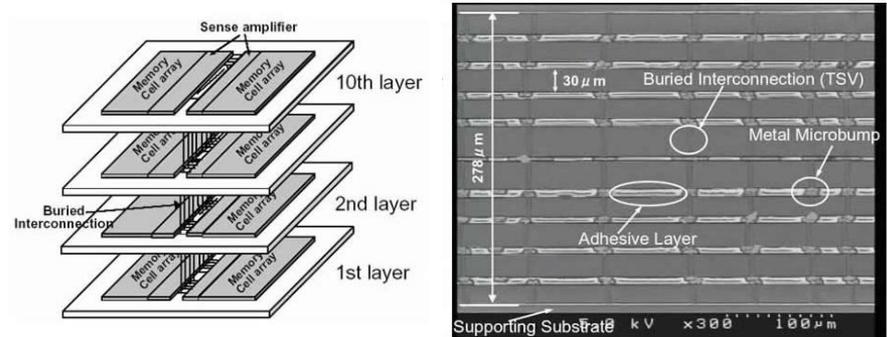


Practical heterogeneous integration historically limited to package level (multi-chip modules) for high-speed RF/mixed-signal applications. Drawbacks:

- I/O parasitics between chips degrade performance.
- Device and interconnect variability issues.
- Excessive latency in high-speed applications

* - 2012 ITRS projection for high-performance S-BGA chip-to-substrate interconnect land pitch using flip chip

Silicon industry is moving to 3D-IC for the same reasons...



Koyanagi, M.; , "The Stacked Capacitor DRAM Cell and Three-Dimensional Memory," *Solid-State Circuits Newsletter, IEEE* , 2008.

3D-ICs in the Silicon Industry:

- Separation between processor and memory limits data bandwidth, creating key bottleneck in processing speed
- 3D-IC structure greatly reduces physical separation, improving I/O bandwidth
- Advanced 3D-ICs have been demonstrated with face-to-face die bonding with $\sim 5\mu\text{m}$ pitch (Kim, et al., ISSC 2012)

Circuit performance limits can be overcome by intimate transistor-level integration



DAHI: Pervasive impact for DoD systems

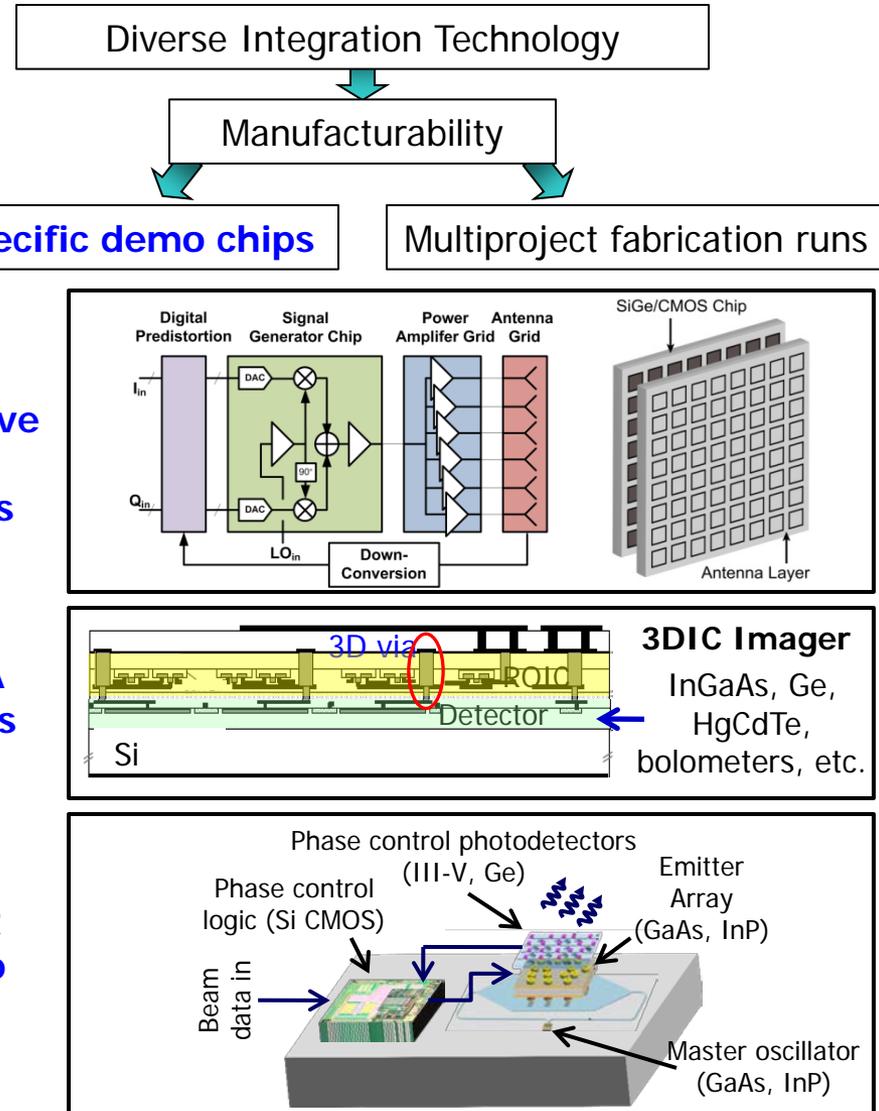
DoD system impacts:

- Radar/EW:
 - Scanning laser radar (LADAR) phased arrays on a chip
 - Phased array radar T/R chip
 - Radar warning receivers
- Communications:
 - Microwave communications transmitters with III-V power components and CMOS-based linearization/waveform processing
 - Laser signal sources with high-speed electronic feedback for coherent communications
 - Integrated Si photonic telecom chips with III-V gain media
- Sensing
 - Fully integrated multi-wavelength (vis./IR) imagers with integrated image processing and high-speed readout circuitry
 - Multi-analyte chem/bio sensing and analysis chips

Microwave comm systems

Multi-λ Imagers

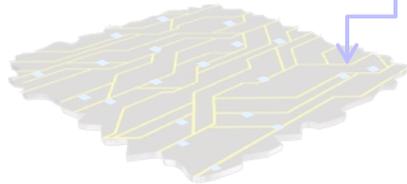
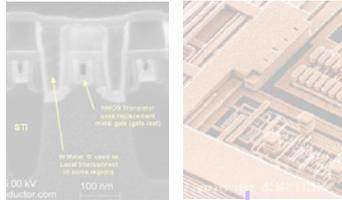
LADAR on chip





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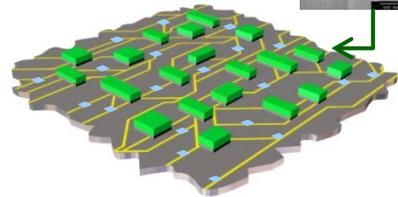
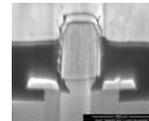
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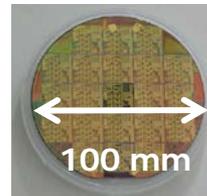
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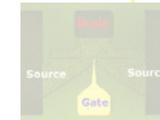
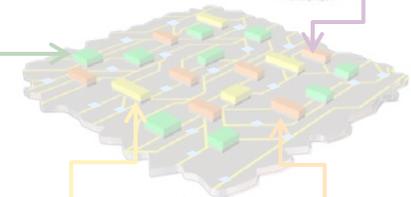
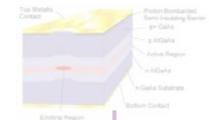
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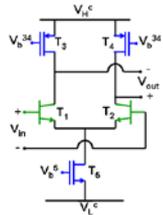
- diverse devices (electronic, photonic, microelectromechanical [MEMS]...) – “best junction for the function”
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of Heterogeneous Interconnects

1000
100
10

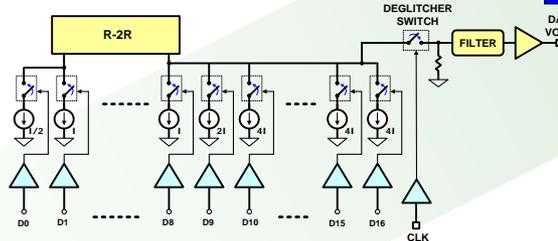
Phase I completed

- ✓ Slew rate $\geq 10^4$ V/ μ sec.
- ✓ Voltage swing ≥ 3 V.
- ✓ DC gain * Unity-gain BW $\geq 10^4$ V/V- GHz.
- ✓ Power ≤ 100 mW.
- ✓ ~5 HBTs, 4 CMOS.
- ✓ ~10 heterogeneous interconnects (HICs).
- ✓ **Differential amplifier**



Phase II underway

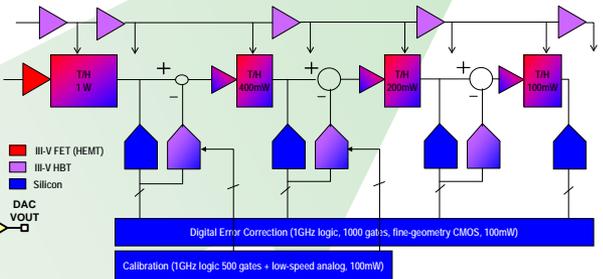
✓ **D/A converter**



- Resolution ≥ 13 bits.
- SFDR ≥ 78 dBc (@ $f_{output} = 1$ GHz).
- Power ≤ 2.5 W.
- ~900 HBTs, 14000 CMOS.
- ~500 heterogeneous interconnects.
- $\leq 5\mu$ m HIC length and pitch.

Phase III (original)

A/D converter



- 16 SNR bits.
- 500MHz bandwidth.
- SFDR ≥ 98 dBc.
- Power ≤ 4 W.
- ~2500 HBTs, 50000 CMOS.
- ~5000 HICs.
- $\leq 5\mu$ m HIC length and pitch.

✓ **Phase I**

Transistor-scale Integration Technology



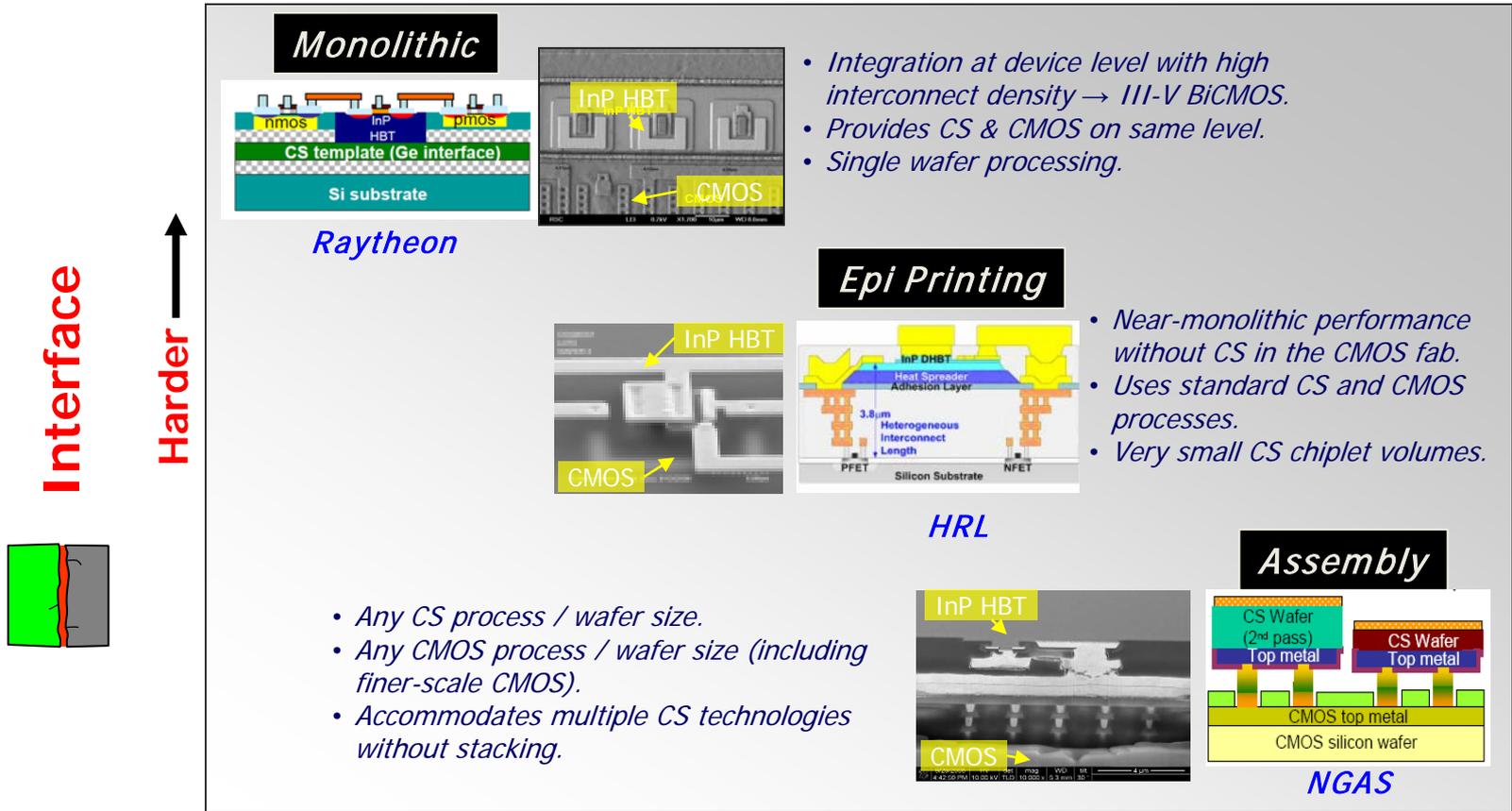
Phase II

Yield Enhancement & Circuit Integration



Phase III

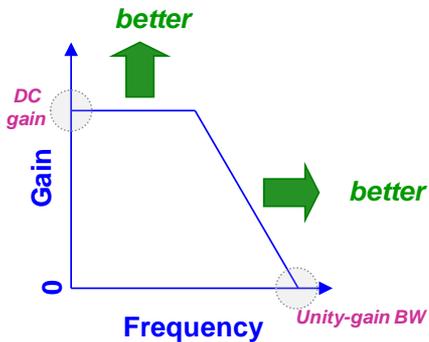
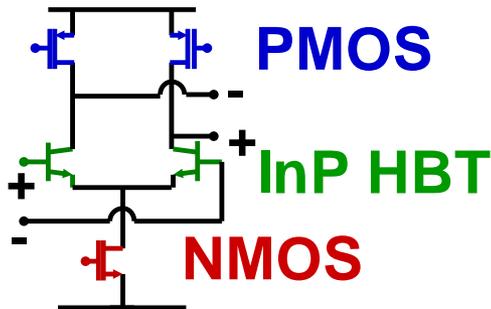
Advanced Circuits



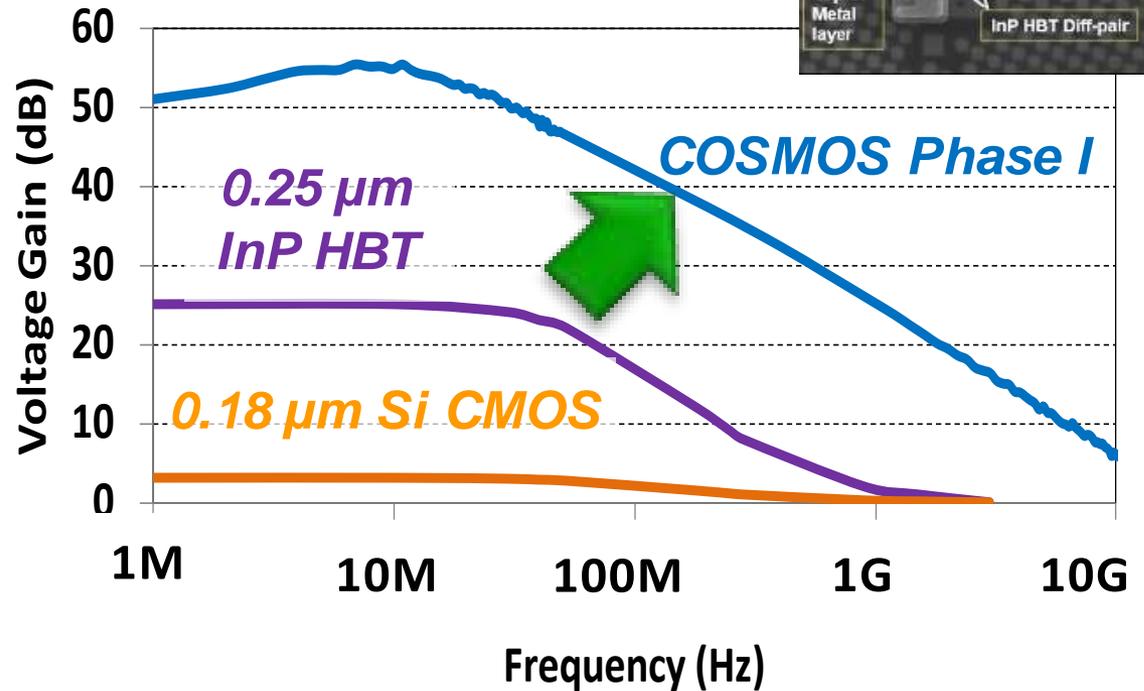
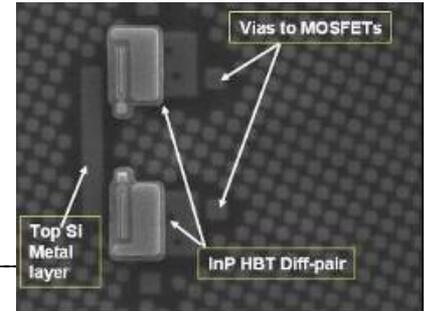


DAHI/COSMOS phase I: differential amplifier

"InP BiCMOS" Technology



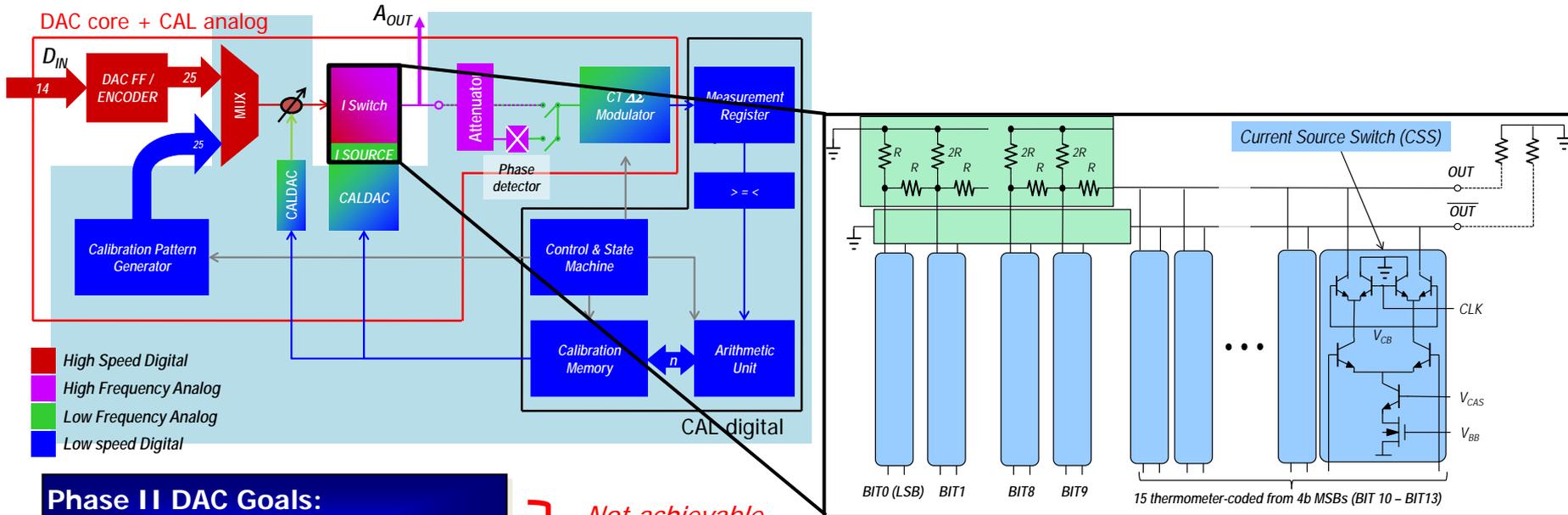
SEM photo of InP HBT from diff-amp circuit on a processed Si wafer



World-record DC gain*Bandwidth Product.



DAHI/COSMOS phase II: high-performance digital-to-analog convertors



Device	Features
InP HBTs	Higher speed, higher V_{br} and intrinsically better transistor matching than CMOS.
Si CMOS	Enables digitally assisted calibration which corrects static and dynamic errors in situ, enhancing dynamic range performance at high speeds.

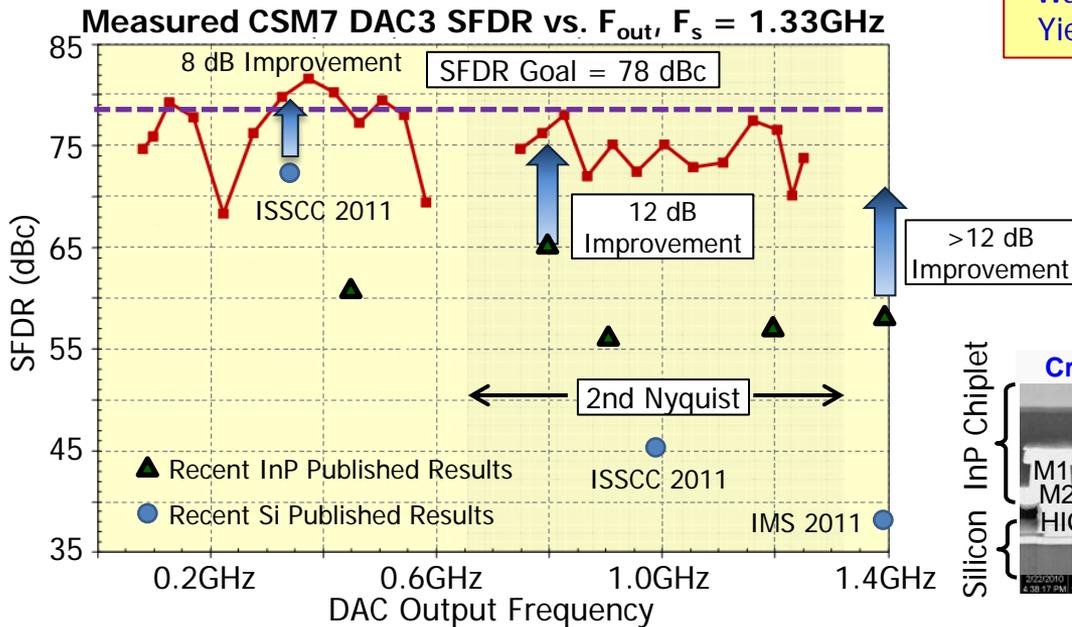
State-of-the-art CMOS-enabled calibration techniques being utilized in COSMOS DACs:

- Static NL (mismatch effects) → tunable current sources, MOS current sources with high r_o , current steering switches, CMOS controlled current source scrambling (DEM)...
- Dynamic NL (signal transitions) → High-speed output deglitchers, CalDAC feedback, timing correction...



NGAS DAHI/COSMOS Phase II Results

- **Achievement:** InP BiCMOS 13-bit, 1.33GHz digital-to-analog converter (DAC) successfully designed, fabricated, and tested
 - Transistor-scale heterogeneous integration with highest complexity to date: 3200 Si MOSFETs, 400 InP HBTs
 - Meets Phase 2 metrics for heterogeneous interconnects (length, pitch, yield), device uniformity
 - Very good DAC and test circuit yield: Measured a fully functional DAC yield of >57% on 2 wafers, each with 78 DAC circuits (4 variants total) on each wafer
 - **DAC Spur-Free Dynamic Range (SFDR) exceeds InP SOA by >12 dB (exceeds Si SOA by >30 dB) in 0.8-1.25GHz range**

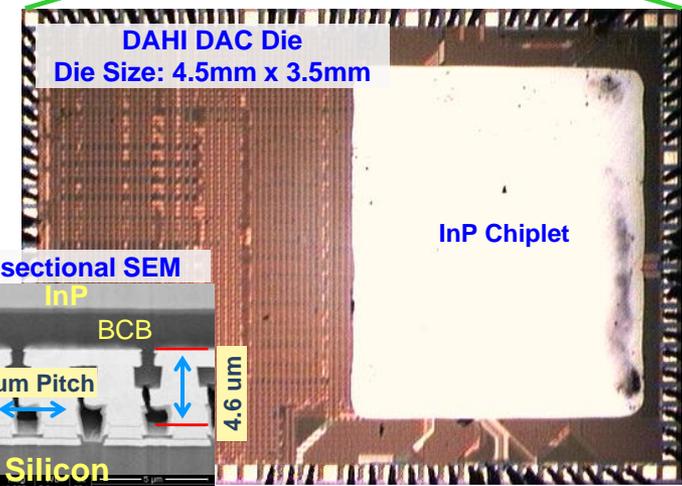
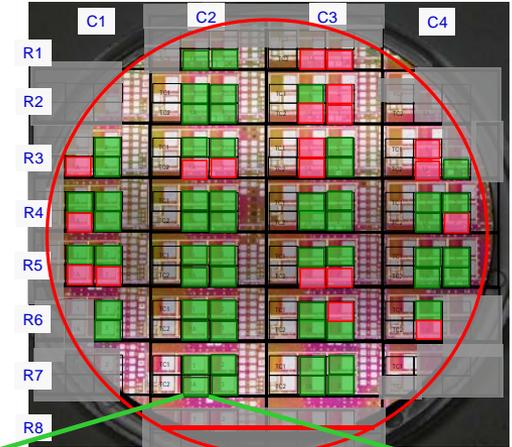


CSM5 COSMOS Wafer Map

- = Probed Circuit, Not Functional
- = Probed Circuit, Fully Functional

Wafer 5-6 DAC Yield = 76.9%

Northrop Grumman

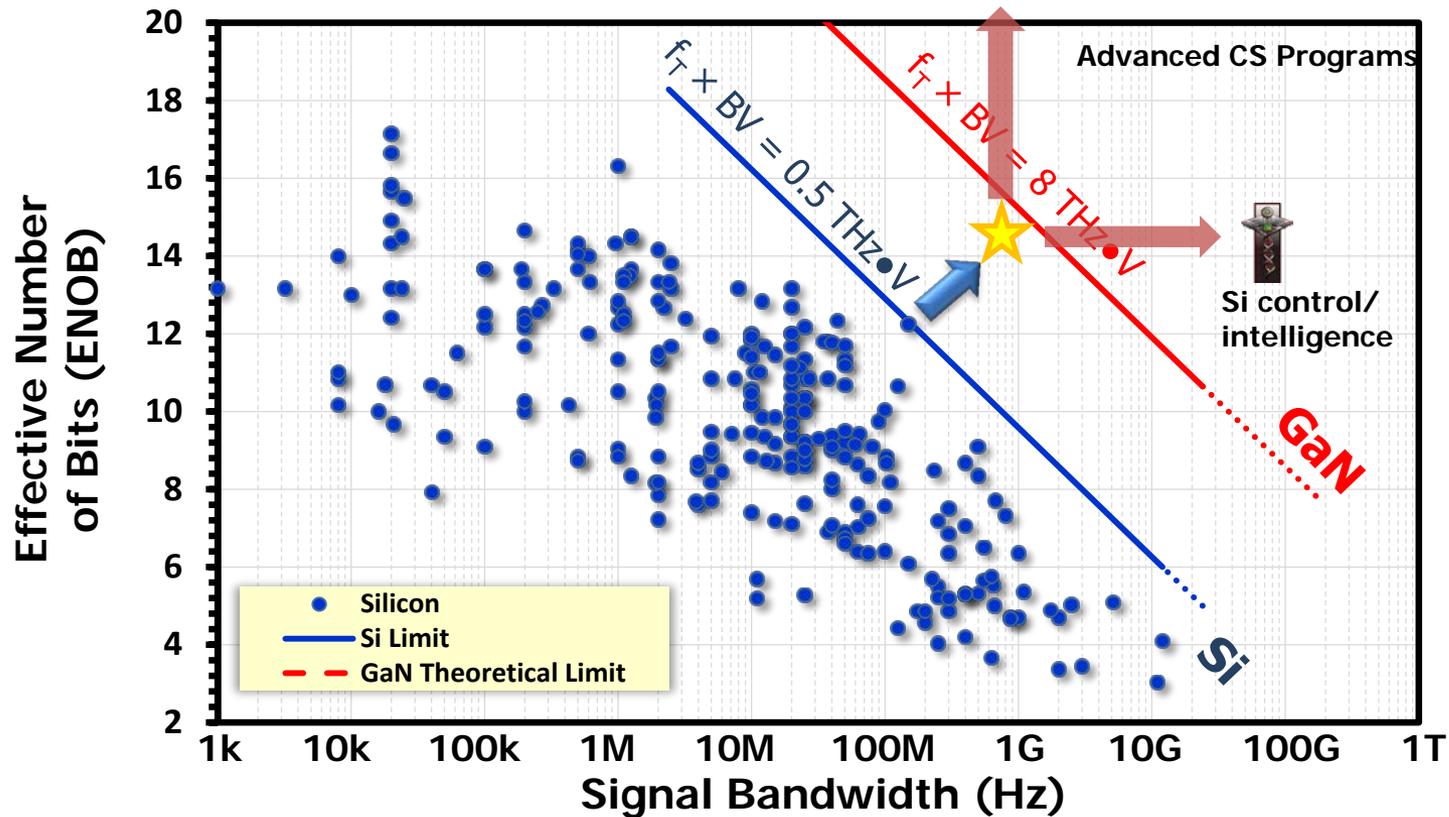


Impact: Enables major improvement in ability to transmit digitally-processed arbitrary waveforms in the GHz range

- Can synthesize very clean advanced waveforms that current SOA DACs cannot (>15x reduction in spurious output power compared to SOA)



The DAHI/COSMOS advantage: surpassing state-of-the-art Silicon ADC performance



Intimate integration of the highest BW and linearity CS devices with complex Si control/linearization/intelligence circuitry enables revolutionary mixed-signal IC performance.



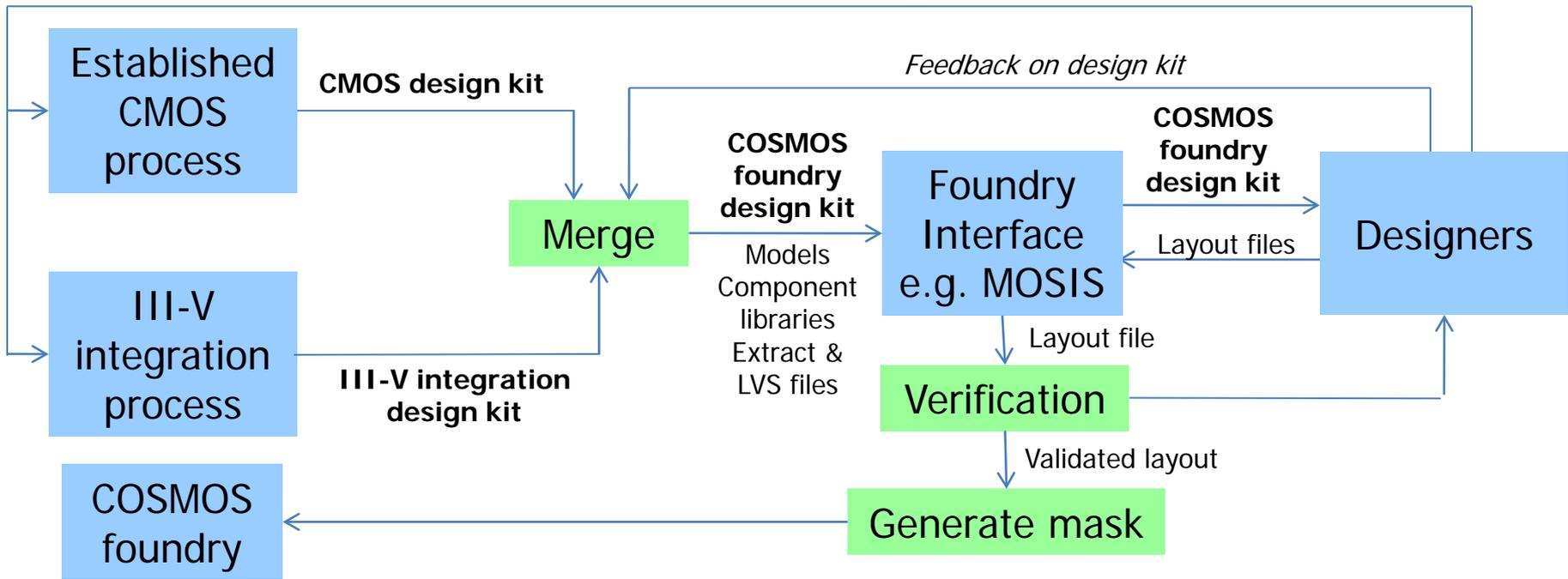
DAHI/COSMOS MPW

HRL Laboratories
Air Force Research Laboratory

Objectives:

- Make DAHI/COSMOS technology available to a wider community of designers.
- Enhance yield, validate the maturity of DAHI/COSMOS process technology.

Feedback on process technology

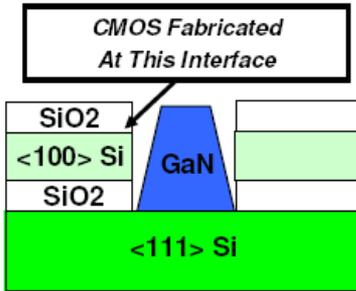


Coming soon to a foundry service near you?

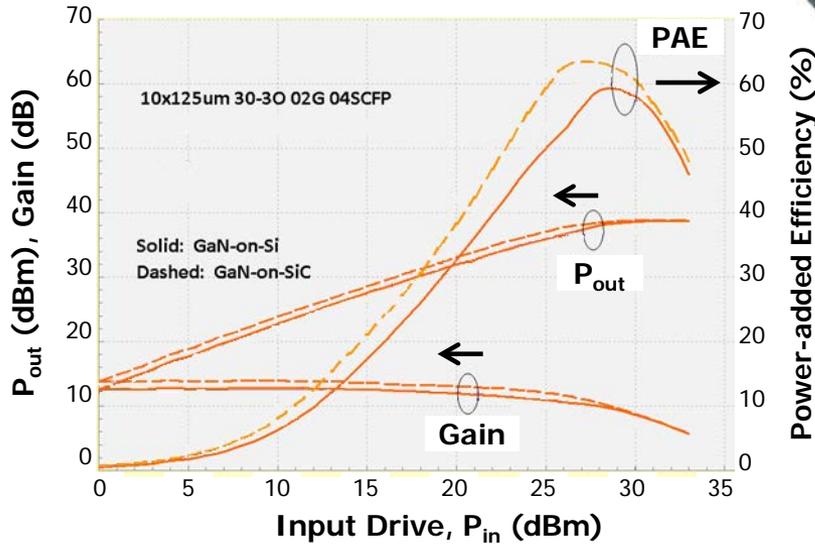


DAHI GaN on Silicon Integration

Raytheon
MIT

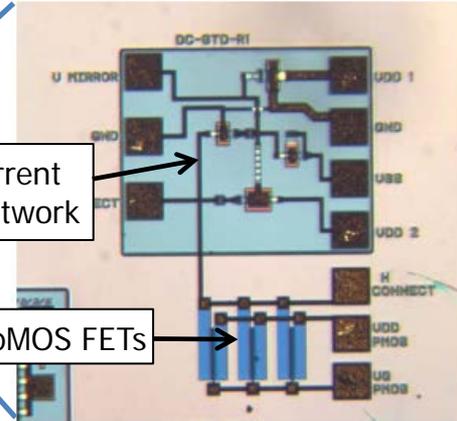
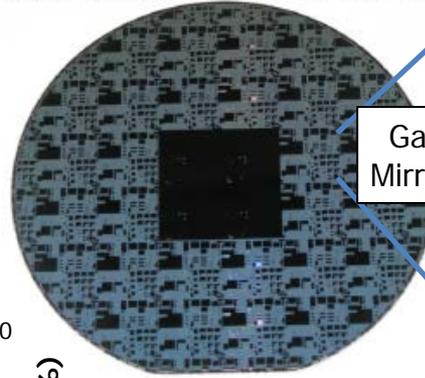


Relatively low MBE GaN growth temperature does not degrade Si CMOS

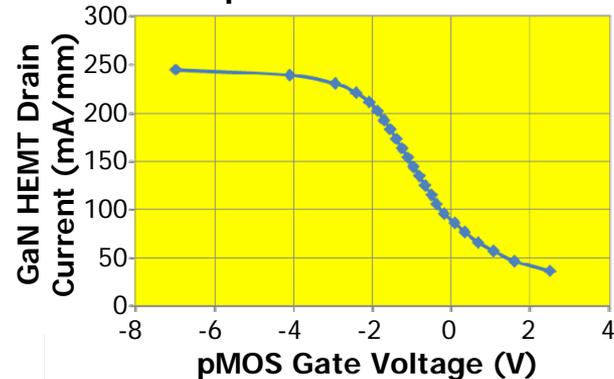


Representative microwave measurements at 10GHz

GaN HEMT growth in windows on SOI



GaN HEMT drain current set by CMOS pFET on same substrate



Demonstrated world's first fully functional heterogeneously integrated GaN HEMT+CMOS RF power amplifier circuit

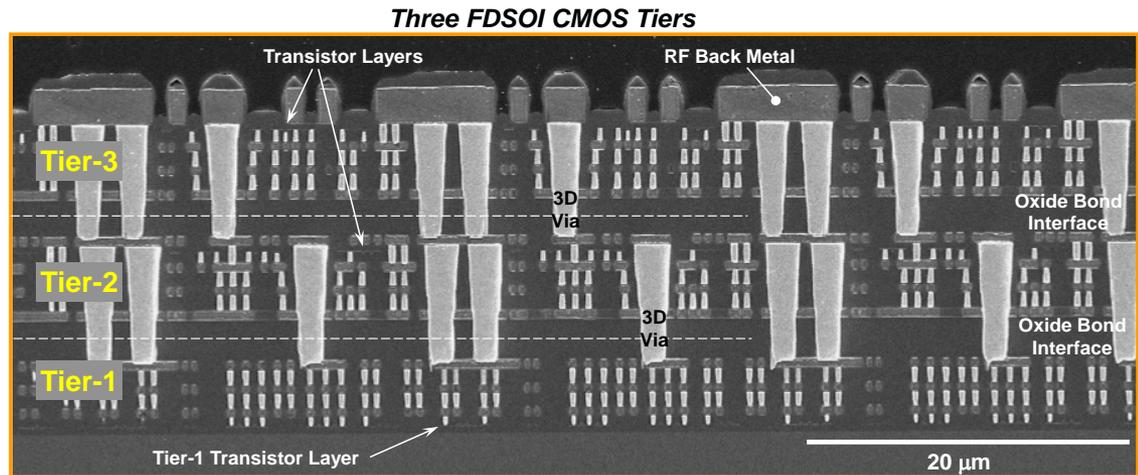
Enables a new class of advanced mixed signal, RF circuits and power conditioning circuits:

- High power digital-to-analog converters (DACs)
- Driver stages for on-wafer optoelectronics
- GaN Power amplifiers with Si linearization circuitry
- Power distribution network in Si electronics



MIT-LL 3D-IC Approach: 3D wafer-level bonding of processed device layers

DARPA-funded effort has developed a 3D heterogeneous integration approach in which processed device "tiers" of different materials are bonded at wafer level.



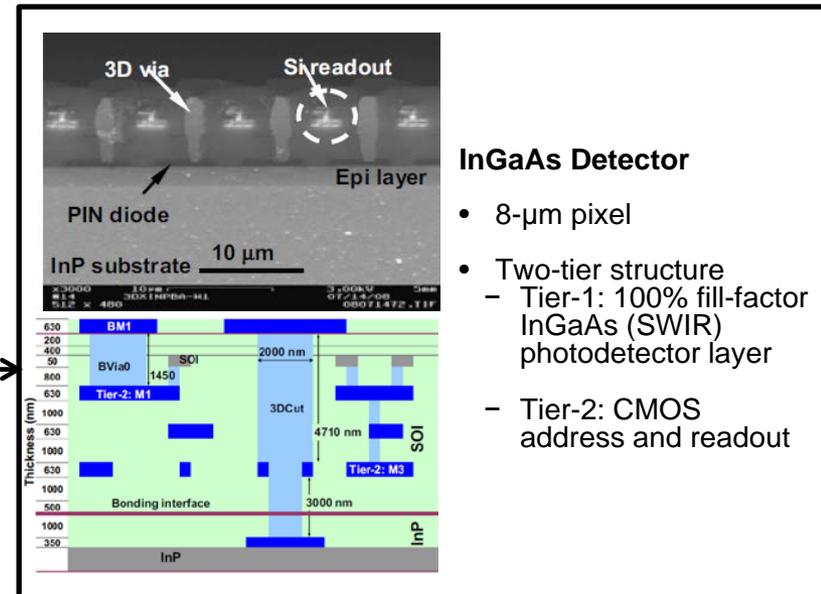
MIT-LL 3D Imager Demonstrations

CMOS Imagers for Daylight Applications

- CMOS Image Sensor (IEEE ISSCC 2005)
- Four-side Abutable CMOS APS (IEEE ISSCC 2009)

Mixed Material / Process Imagers

- GmAPD Laser Radar (IEEE ISSCC 2006)
- InGaAs Detector (IEEE 3DIC 2009)



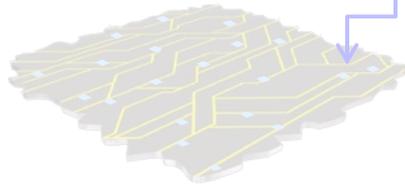
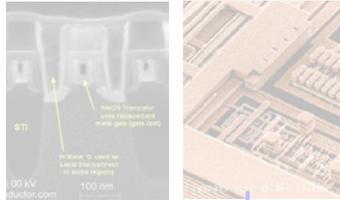
InGaAs Detector

- 8-μm pixel
- Two-tier structure
 - Tier-1: 100% fill-factor InGaAs (SWIR) photodetector layer
 - Tier-2: CMOS address and readout



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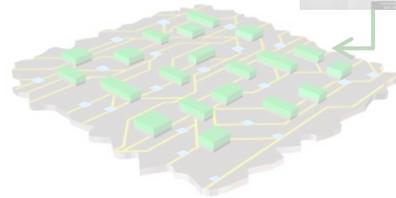
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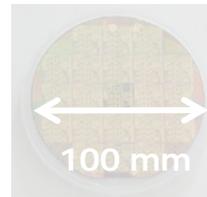
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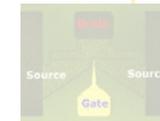
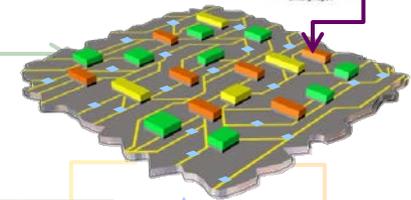
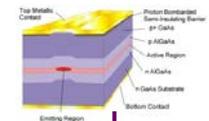
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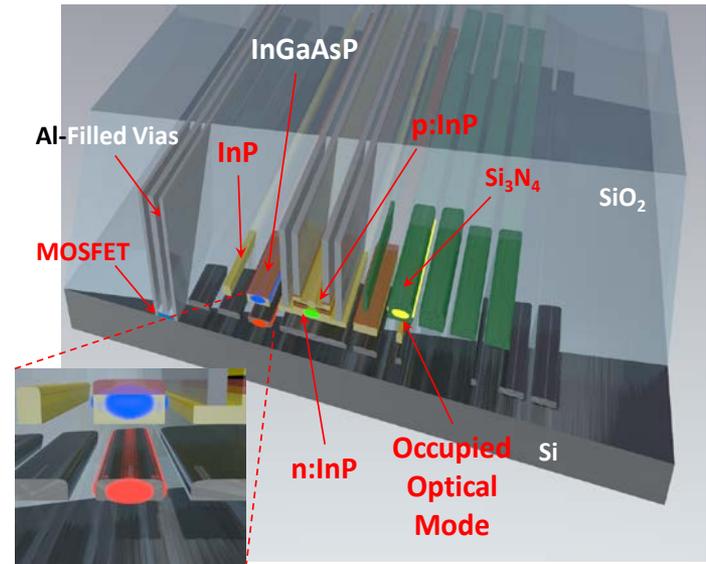
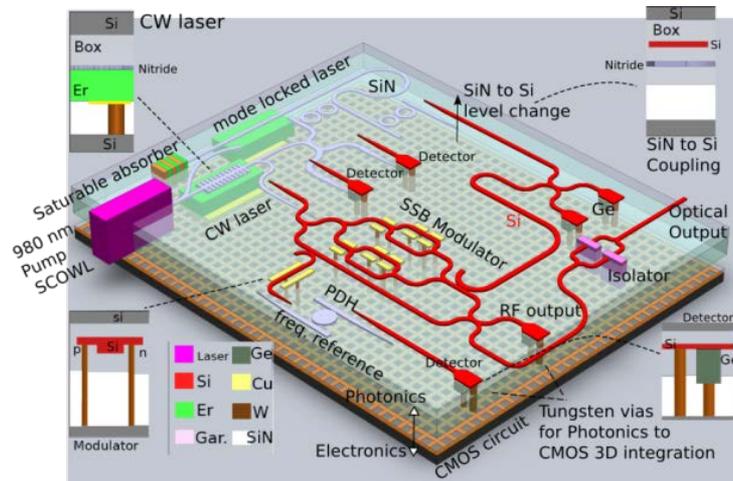
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New DAHI Thrust: Electronic-Photonic Heterogeneous Integration (E-PHI)

Goal: to develop the necessary technologies, architectures, and design innovations to enable novel chip-scale electronic-photonic/mixed-signal integrated circuits on a common silicon substrate.



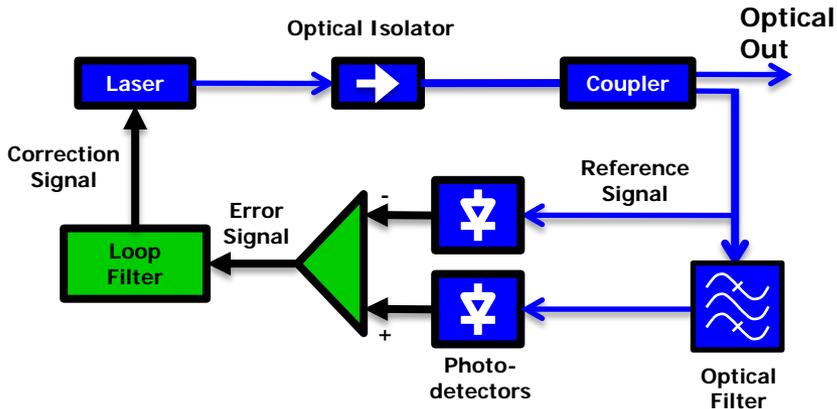
Technical Areas:

- I. Heterogeneous Electronic-Photonic Integration Process and Device Technologies
- II. Heterogeneously Integrated Electronic Photonic Architectures
- III. Demonstration Microsystems
 - Demonstration A: Laser Sources
 - Demonstration B: RF Opto-Electronic Signal Sources
 - Demonstration C: Other Advanced Electronic-Photonic Integrated Circuit Demonstrators

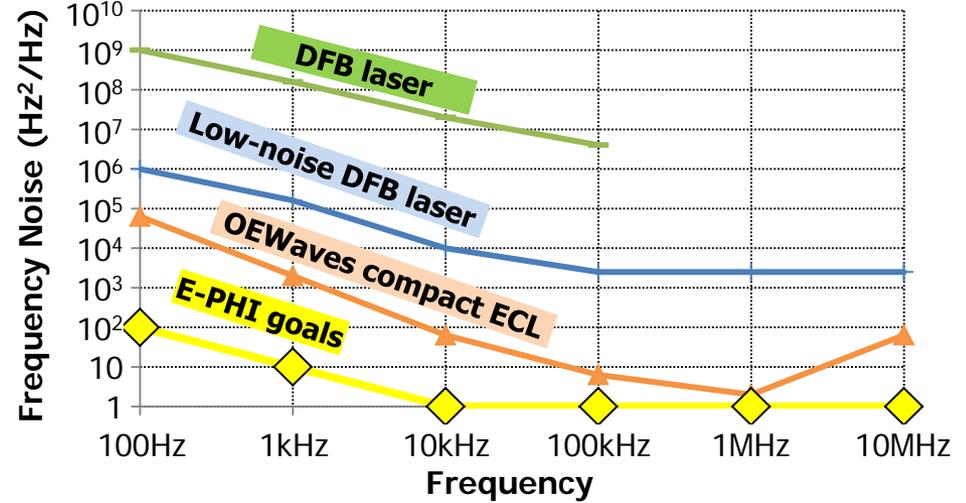


Low noise sources

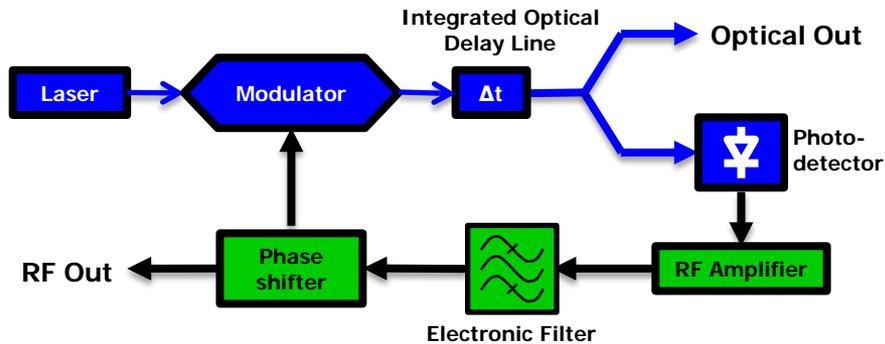
CW laser sources



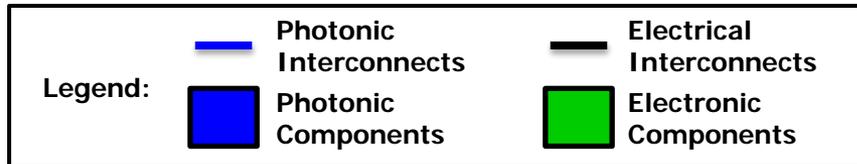
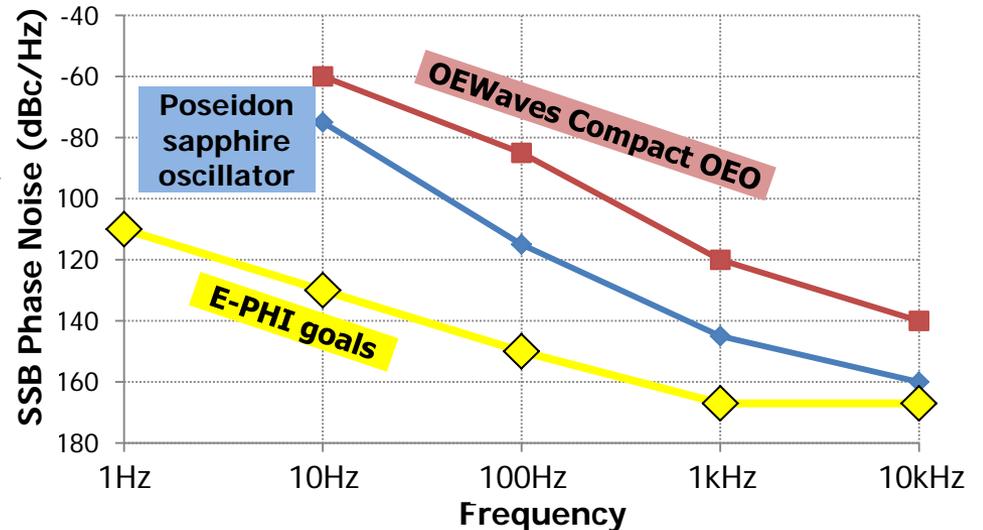
Freq. Noise vs. Freq. – “Chip-scale” CW Laser sources



Opto-electronic signal sources



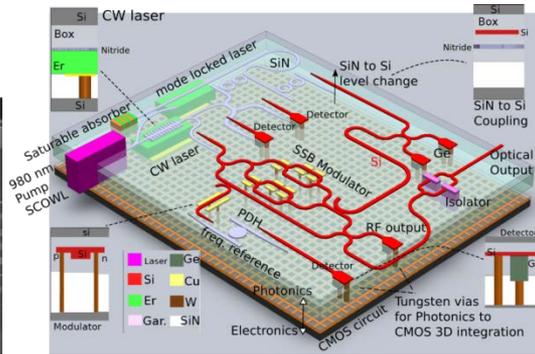
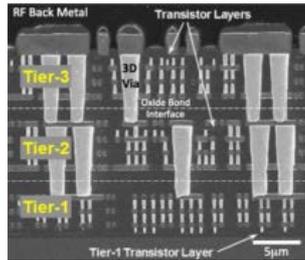
Oscillator Phase Noise (normalized to 10GHz) vs. Freq.





E-PHI Team Summaries: Technical Area I

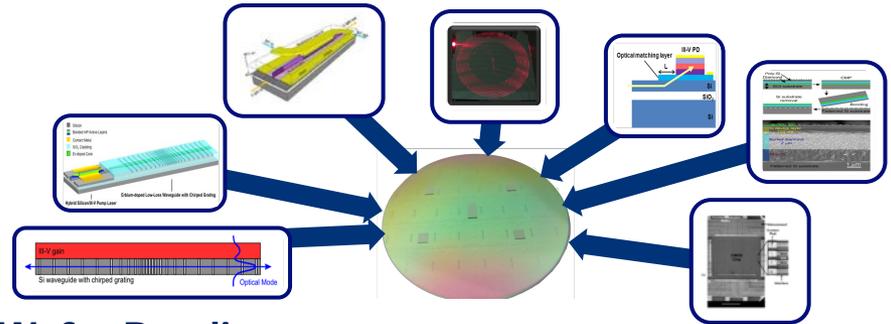
MIT



3D Photonic Electronic Integration

- Combine the Si photonics platform of CNSE with the 3D integration of MIT Lincoln Labs.
- Use butt coupled III-V pump lasers to drive ErYb-doped gain regions.

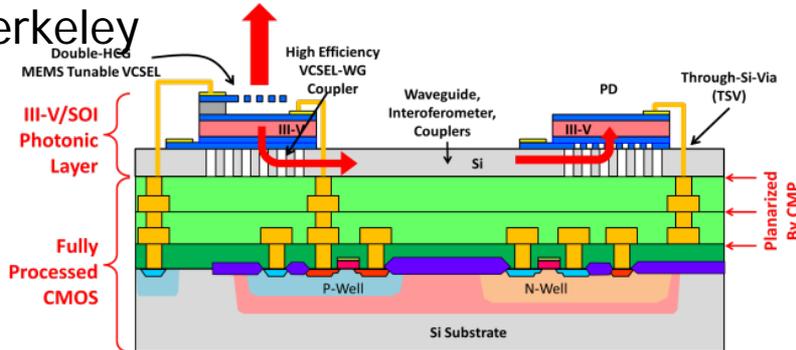
Aurion



Wafer Bonding

- Different optical materials are wafer bonded to a Si substrate, and evanescently coupled to the waveguides.
- CMOS electronics included as a chiplet on the optical wafer.

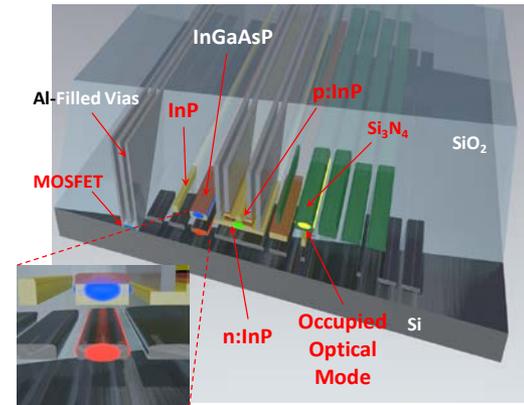
UC Berkeley



CMOS First Wafer Bonding

- Two step bonding of photonics layers are bonded to fully processed CMOS wafer. CMOS to SOI and III-V to SOI.
- Grating coupling between III-V active regions and the Si photonics layer.

UCSD



InPOI

- Wafer scale bonding of InP to SOI to produce InPOI.
- Adiabatic coupling between multiple functionally different photonic layers.



DAHI Foundry Technology Thrust

BAA Overview



Some important BAA 12-16 guidance

1. Read the BAA.
2. Read it again.
3. Read it a few more times.



BAA Overview Information

- **Funding Opportunity Title** – Diverse Accessible Heterogeneous Integration (DAHI) Foundry Technology
- **Funding Opportunity Number** –DARPA-BAA-12-16

- **Dates:**

- Posting Date: March 29, 2012
- Proposer's Day: April 18, 2012.
- Proposal Abstract Due Date: May 9, 2012
- Proposal Due Date: July 9, 2012

- **Concise description of the funding opportunity:**

The goal of the DAHI Foundry Technology BAA is to develop advanced heterogeneous integration processes, allowing diverse material systems and device technologies to be tightly integrated on a common silicon substrate. The DAHI program thrust aims to establish a manufacturable foundry technology to provide accessibility to a broad community of designers for innovative circuit or microsystem designs.



- **Total amount of money to be awarded:**

It is anticipated that total funding in the range of **\$80M-\$100M** will be awarded across Technical Areas I, II, and III discussed in this BAA, and **the majority of this funding is expected to be allocated in Technical Area II**. The actual amount of resources made available under this BAA will depend on the quality of the proposals received and the availability of funds.

- **Type of funding to be awarded:**

Technical Area I and III efforts may be conducted as fundamental or non-fundamental research (6.1, 6.2, or 6.3 funding is available). However, Technical Area II efforts are expected to be conducted as non-fundamental research (6.2 not on a University campus or 6.3 funding only).

- **Anticipated individual awards** – Multiple awards anticipated across Technical Areas I, II and III for 36-48 month efforts.

- **Email:** DARPA-BAA-12-16@darpa.mil

- **Full BAA Listing:** <https://www.fbo.gov/spg/ODA/DARPA/CMO/DARPA-BAA-12-16/listing.html>



BAA General Description

- Seeking proposals for the development of heterogeneous integration technologies and methodologies, resulting in process modules for a wide array of materials and devices coexisting on a silicon wafer.
 - Ultimate goal is integration of **at least 3 heterogeneous device technologies** on **Si wafers $\geq 200\text{mm}$ in diameter**, with **transition to a sustainable foundry offering** at end of this program thrust
 - Focusing on integration of compound and alloy semiconductor-based electronic devices, passive components, MEMS structures/sensors, and/or thermal management structures, with silicon CMOS/SiGe BiCMOS transistors or circuits.
- **Process modules for photonic devices are not sought in this BAA since analogous efforts have been initiated under BAA 11-45, Electronic-Photonic Heterogeneous Integration (E-PHI).**
 - However, DARPA ultimately seeks incorporation of E-PHI process modules within the overall DAHI program technology base where feasible.
- **As always, specifically excluded is research that results in evolutionary improvements to existing state-of-the-art.**



Technology Diversity

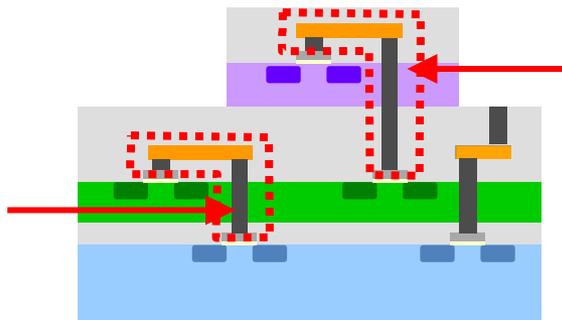
- Will develop device-level heterogeneous integration of at least three different microsystem technologies on a single silicon-based chip
 - Note that the silicon device technology itself, e.g. bulk CMOS, Si bipolar, SOI CMOS, SiGe BiCMOS, etc. counts as **one** of the three technologies.
 - **Process modules already available in silicon CMOS/BiCMOS technologies** (for example, available CMOS-MEMS integration processes) are considered to be in the category of an already existing silicon base technology, and thus **will not count as novel heterogeneous integration technologies** for the purposes of this BAA.
- In the **first phase** of the DAHI foundry thrust, a base technology with three different device types on silicon is to be demonstrated, e.g. a phase structure adding one new heterogeneous technology each phase would not be of interest.
- Seeking integration of technologies that provide maximum **performance** benefit to DoD system needs.
- At the end of the thrust, Tech Area II team(s) are expected to provide a scalable DAHI process integrating the initial distinct technologies, but also support addition of additional process modules that may be developed subsequent to effort based on circuit designer and application needs



Integration Proximity

- The integration proximity goals for the DAHI Foundry Technology BAA are to achieve both of the following:
 - -3dB bandwidth of at least 20GHz across a heterogeneous interconnect (with appropriate G/S, G/S/G, or other appropriate interconnect structure)
 - Delay of less than 5 picoseconds (note that this delay should include the parasitics of the heterogeneous devices that are being connected).
- Both metrics should be measured across interconnects between one of the heterogeneous device technologies and the base silicon device technology, or between two different non-base silicon device technologies

Interconnect between one heterogeneous device and base Si technology



Interconnect between two different heterogeneous non-base silicon device types

- **These metrics are intended for high-speed device integration and do not necessarily apply to all devices of interest (e.g., certain MEMS structures)**
- These metrics may be directly measured on specific test structures, which are independent of more complex demonstration circuits. Note that the two metrics do not have to be measured on the same structure (for instance, delay could be measured using a ring oscillator structure, while a passive probed structure could be used to measure bandwidth).



Foundry Capability

- DAHI Foundry Technology envisions the development of diverse heterogeneous integration on at least 200mm Si wafers by either:
 - 1) Directly integrating diverse components on $\geq 200\text{mm}$ wafers, or
 - 2) Fabricating different DAHI process modules on alternate substrates and subsequently integrating or assembling the diverse component technologies onto the final substrate.
- Process does not need to be completely resident in the silicon fabrication line, as long as the overall process flow results in diverse integration and close proximity on $\geq 200\text{mm}$ Si substrates.
- Scalability (both in terms of device dimensions as well as potential for production volume) is an important consideration for both the silicon and the other materials.
 - **DARPA is particularly interested in processes that leverage deeply scaled CMOS technology and the most advanced scaled non-silicon devices, as appropriate.**
- Another important element is the development of complete process design kits that provide accurate models of all active devices, passive components, and heterogeneous interconnects.
 - Offerors should provide a plan for third party access to the physical fabrication capability, including releases of physical models, design kits, etc., as appropriate and needed.
 - Also of particular interest is foundry support for design capabilities including thermal simulation, process corners for Monte Carlo simulation, DRC rule-checking, and parasitic extraction.



Technical Areas of Interest

Technical Areas:

I. DAHI Process Development

- Development of heterogeneous integration processes that can integrate **at least three** different component technologies

II. DAHI Foundry Establishment

- Development of a foundry capability on $\geq 200\text{mm}$ wafers to provide diverse accessible heterogeneous integration process technology on a multi-user basis

III. DAHI Circuit Design Innovation

- Exploration of novel circuit design techniques and methodologies that enable revolutionary DAHI circuit architectures
- May include development or augmentation of design/simulation tool flows necessary to enable or optimize DAHI design environments.

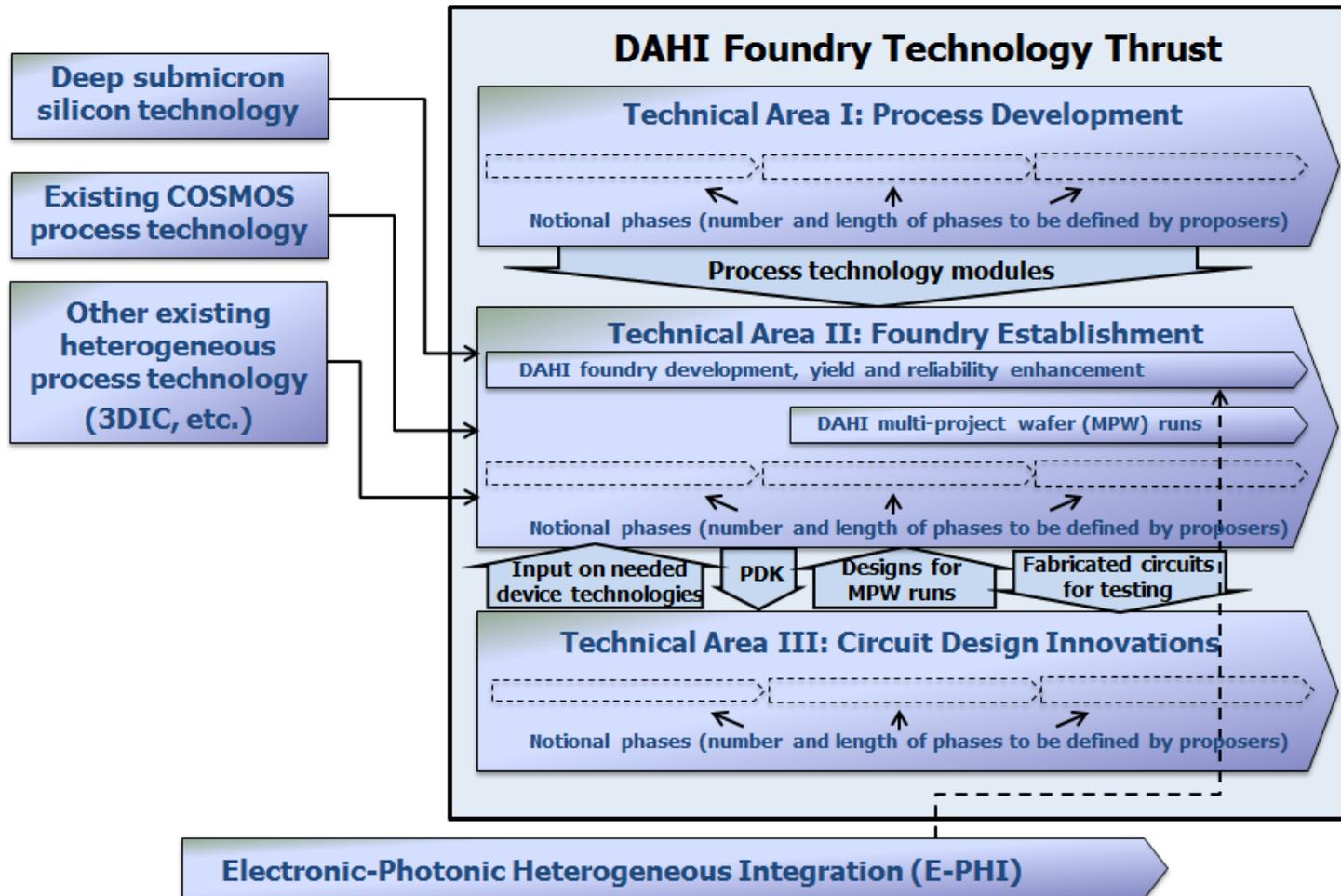
- *Proposers are strongly encouraged to focus on only one of three technical areas of interest.*

- If the proposers decide to propose to more than one technical area in a single proposal, the technical proposal should clearly address the requirements of individual technical areas. Such proposals will be strictly held to the abstract and full proposal page limitations.
- Both technical and cost proposals should be atomically structured so that individual Technical Areas (and tasks within Technical areas) may be selected independently of one another.

- Interaction among performers in different technical areas is expected in order to realize a unified thrust towards the overall DAHI vision.



DAHI Foundry Technology: Technical Area Interactions



The proposers should propose their program phases and phase durations as well as associated intermediate technical milestones. The total length of the proposed efforts is expected to range between 36 and 48 months.



Technical Area I: Process Development

- The DAHI Process Development area focuses on developing heterogeneous integration processes that can integrate at least three different component technologies as described above.
- The proposed approaches under this Technical Area are **NOT specifically required to be demonstrated on ≥ 200 mm wafers**, but should have practical technical paths and plans to integrate the process module with or onto at least 200 mm diameter silicon wafers.

Technical Area I metrics:

Metrics	Program Goals
Numbers of Heterogeneously Integrated Device Technologies ^a	≥ 3 different technologies
Heterogeneously Integrated Device Performance ^b	$\geq 90\%$
-3dB Heterogeneous Interconnect Bandwidth ^c	≥ 20 GHz
Heterogeneous Interconnect Electrical Delay ^d	≤ 5 psec
Wafer Size	Proposer-defined ^e
Demonstration Circuit(s) ^f	Proposer defined circuit(s) which demonstrate simultaneous integration of all (≥ 3) proposed technologies on a single silicon substrate/chip.
Demo Circuit Yield	$\geq 50\%$ functional yield of proposed demonstration circuit(s) meeting $\geq 90\%$ design performance.
Design Kits	Models, structures, cores, etc., compatible with industry standard electronic design automations (EDA) tools with verification and parasitic extraction capabilities. Able to be evaluated by the government.



Technical Area II: Foundry Establishment

- Focuses on developing a complete foundry capability to provide diverse and accessible heterogeneous integration processes for DoD users.
- Only 1-2 awards are anticipated in Technical Area II.
- In Technical Area II, the proposer must develop the DAHI technology **on ≥ 200 mm diameter silicon wafers** and provide the foundry service through multiproject wafer (MPW) runs for government-selected design teams during the DAHI program (these may be Technical Area III performers).
The proposer is expected to either:
 - 1) Directly develop the DAHI processes on ≥ 200 mm silicon wafers and provide the foundry service, or
 - 2) Serve as the integrator of the DAHI process modules to develop techniques to tightly combine DAHI process modules on the ≥ 200 mm silicon wafers.
- The proposers of Technical Area II should plan to provide **no less than two MPW runs** throughout the development of the DAHI Foundry Technology thrust, and **fabrication for the first MPW run should begin no later than 30 months after the award of contract**. A minimum of 40 chips should be provided to each design team.



Technical Area II: Foundry Establishment *Metrics*

Metrics	Thrust Goals
Numbers of Heterogeneously Integrated Device Technologies ^a	≥ 3 different technologies
Heterogeneously Integrated Device Performance ^b	≥ 90 %
-3dB Heterogeneous Interconnect Bandwidth ^c	≥ 20 GHz
Heterogeneous Interconnect Electrical Delay ^d	≤ 5 psec
Wafer Size	≥ 200 mm diameter silicon wafers for all MPW runs.
Yield Test Vehicle Circuits	Proposer defined yield test vehicle circuits to enable detailed yield analysis of overall process flow as well as individual process modules ^e .
Heterogeneous Integrated Circuit Complexity	Factor of 100 increase in complexity of yield test vehicle from beginning to end of thrust ^f .
Within-wafer Yield Test Vehicle Circuit Yield	≥50 % functional yield of proposed yield test vehicle circuit(s) meeting ≥ 90% design performance ^g .
Within-lot Yield Test Vehicle Circuit Yield	≥50 % functional yield of proposed yield test vehicle circuit(s) meeting ≥ 90% design performance ^g . The functional yield is calculated from 6 wafers which contain at least 20 yield monitoring circuits per wafer.
Heterogeneous Device and Interconnect Reliability	Mean time-to-failure of heterogeneous devices and interconnects >10 ⁶ hours.
Design Kits	Models, structures, cores, etc., compatible with industry standard electronic design automations (EDA) tools with verification and parasitic extraction capabilities. Able to be evaluated by the government.
Foundry Capability	At least two multiproject wafer (MPW) runs with ≥6 full wafers completing fabrication per run and ≥ 40 chips delivered back to each design team per run. Fabrication for the first MPW run should begin no later than 30 months after the award of contract.



Technical Areas I and II:

Heterogeneously Integrated Device Performance Metric

Metrics	Thrust Goals
Heterogeneously Integrated Device Performance ^b	≥ 90 %

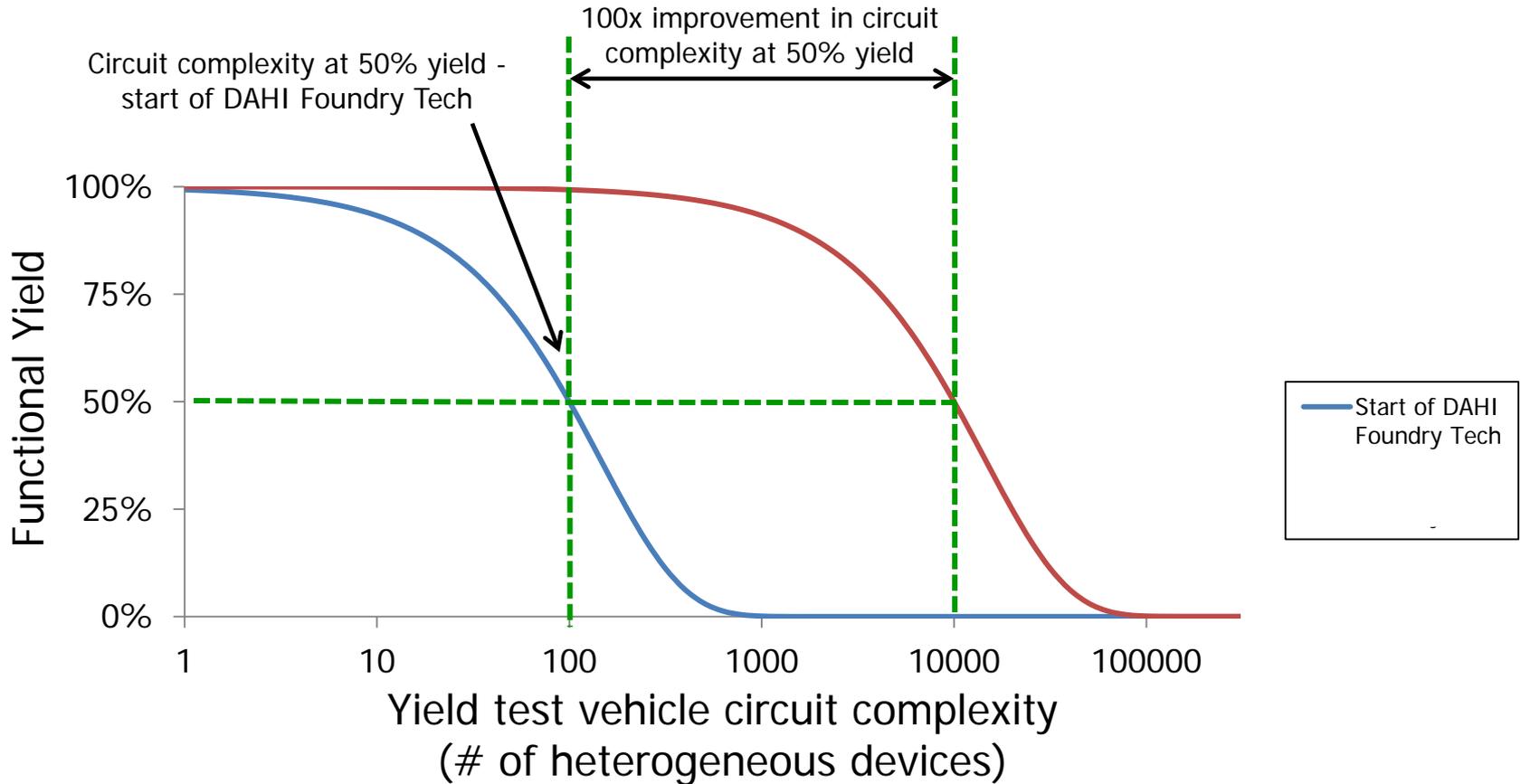
b. The ratio of the peak performance of heterogeneously integrated devices to that of the same devices fabricated on a native substrate.

- Proposers must propose and justify appropriate device metrics to establish the performance of the heterogeneously integrated devices.
- May be appropriate to include more than one metric per device type for this purpose.
- It is also anticipated that **adequate device thermal management** will be required for high-speed electronic devices to achieve their peak performance metric (such as f_T or f_{max} of transistors).
- The “native” substrate may be the industry standard substrate used for a particular device type (e.g. SiC for GaN transistors)



Technical Area II: *Circuit Complexity Metric*

Metrics			Thrust Goals
Heterogeneous Complexity	Integrated	Circuit	Factor of 100 increase in complexity of yield test vehicle from beginning to end of thrust ^f .



Yield test vehicle must include all (≥ 3) device technologies



Technical Area II: Foundry Establishment *Specific Issues*

- Technical Area II **full proposals** *may* also be evaluated through site visits by members of the government review team in order to fully understand and validate the proposer's capability to execute their proposed Technical Area II efforts.
- Selection for a site visit does NOT imply selection for negotiation for a potential award.



Technical Area III: Circuit Design Innovation

- This Technical Area focuses on exploring innovative DAHI circuit design techniques and methodologies.
- It is envisioned that work in this area will begin in parallel with process technology work.
- During the initial phase of the efforts in this Technical Area, participants will be expected to provide input to Technical Area I and II participants regarding the device/material technologies that are of greatest interest to be included in the DAHI foundry offering.
- Seeking innovations in design that can both guide the needs of the technology and allow the technology to realize microsystem performance that cannot be achieved by any one material/device technology alone.
- Simulation results of heterogeneously integrated circuits from Technical Area III will be leveraged by the government to provide technical input and feedback to Technical Area I & II performers.
- Design tool augmentations or developments for future DAHI technology design environments are encouraged.

Metrics	Thrust Goals
Numbers of Heterogeneously Integrated Device Technologies used in a single circuit design ^a	≥ 3 different technologies
DAHI Circuit(s)	Performer defined
Circuit Performance	Improved or unique circuit performance which cannot be achieved by homogeneous technologies. ^b



Some further abstract/proposal guidance

- Abstracts are NOT required for full proposal submission, but are strongly encouraged in order to obtain feedback on proposed ideas.
- Note separate abstract format described in the BAA (NOT the summary section of the full proposal)
- Abstracts/proposals should clearly identify intermediate technical milestones for each phase. **The proposed milestones should be quantifiable and measurable and should not simply reflect the completion of task elements. All intermediate technical milestones, as well as end-of-thrust goals, should be listed in a table.**
- For TA I & II, **provide sufficiently detailed descriptions or figures to clearly depict the proposed process flow to heterogeneously integrate ≥ 3 diverse technologies.** Clearly define the proposed heterogeneous integration technology approach, its development schedule and intermediate technical milestones, and mitigation approaches and their development plans.



Good Luck! (Q&A scheduled at the end of the day)
